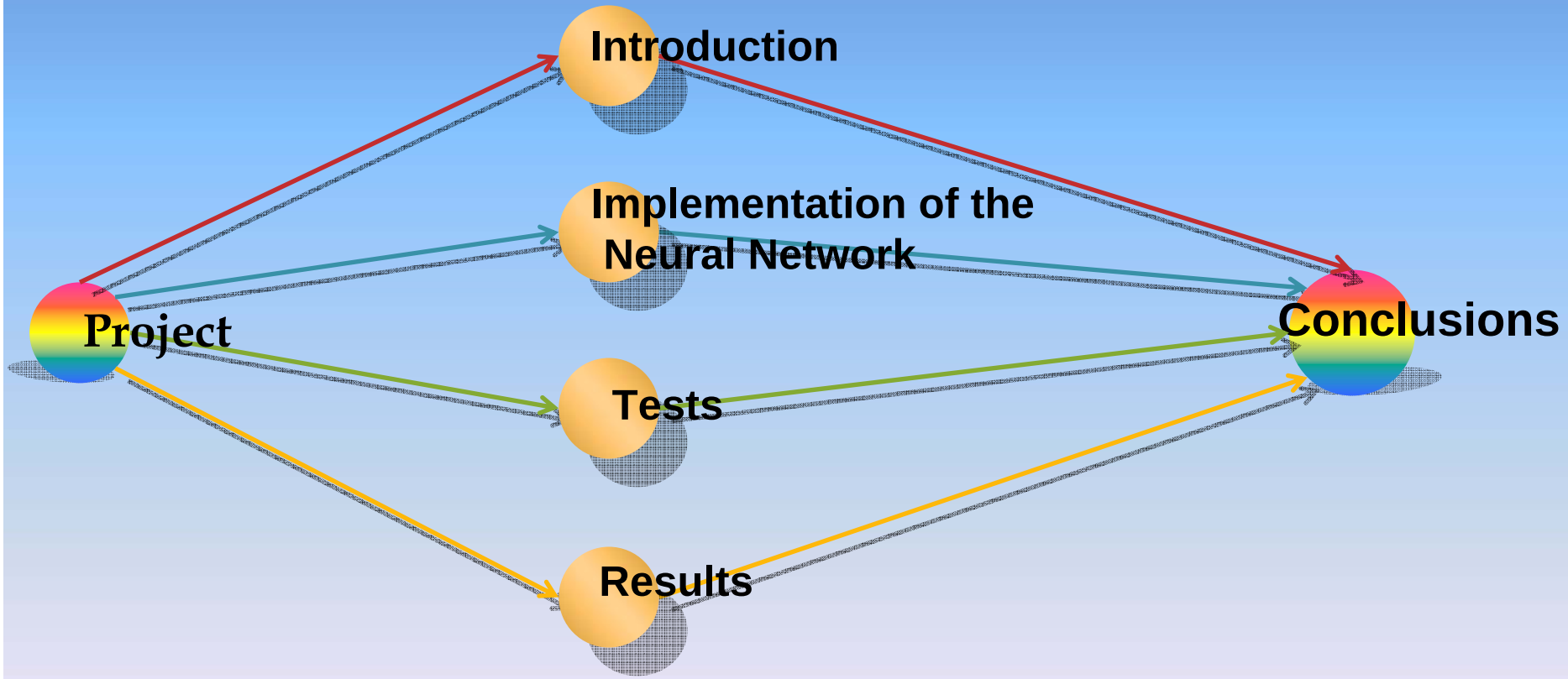
Universidade da Madeira

Hardware Implementation of an Artificial Neural Network with an Embedded Microprocessor in a FPGA

SUMMARY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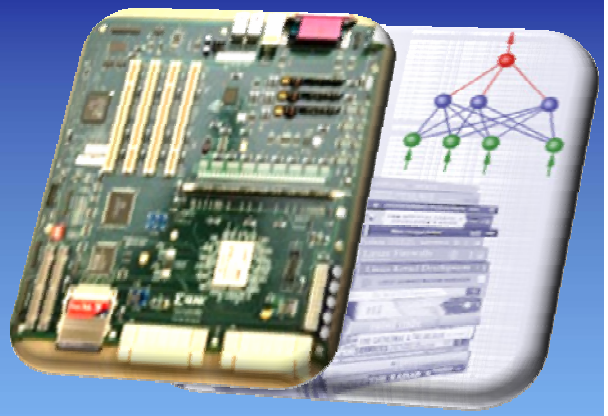
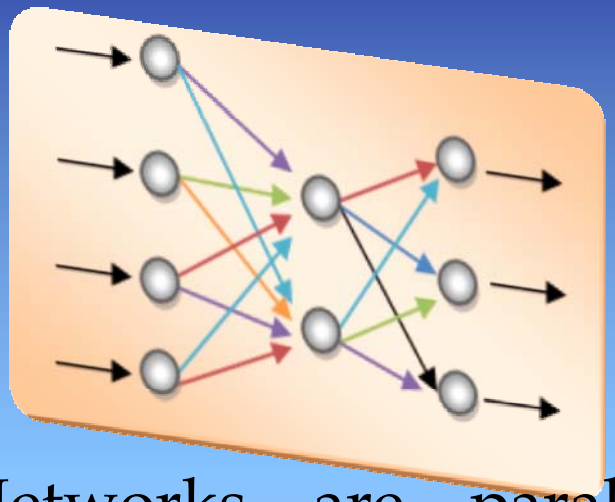
INTRODUCTION



- The OBJECTIVE of this PROJECT

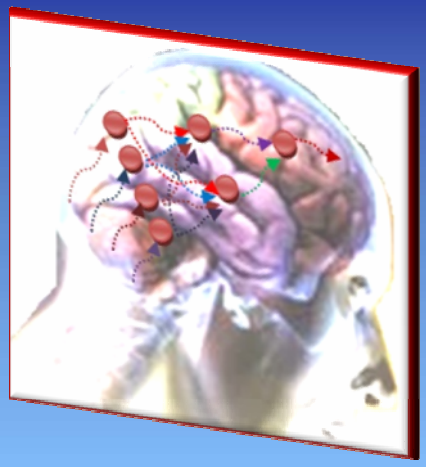
  is the hardware implementation of a neural network with an embedded microprocessor, which can be a valuable resource for many scientific areas as Applied Sciences and Health Sciences.

INTRODUCTION



- The Artificial Neural Networks are parallel distributed systems, since they have the capacity to receive several inputs at the same time and to distribute these inputs in an organized manner.

INTRODUCTION

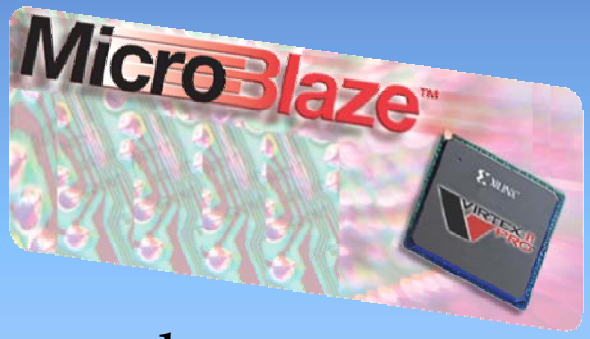


- The implementation of an Artificial Neural Network will have to supply a signal to the output of the system that will activate the coupled components, resembling what happens in the Biological Neural Network.

IMPLEMENTATION of the NEURAL NETWORK

- HARDWARE PLATFORM
  - To carry out this implementation, the device FPGA Virtex II Pro XC2VP30 was used with a MicroBlaze soft core microprocessor, from Xilinx.

IMPLEMENTATION of the NEURAL NETWORK



- The MicroBlaze has advantages such as:
  - simplicity in the design,
  - high reusability and
  - easy integration with other technologies.

IMPLEMENTATION of the NEURAL NETWORK

- IMPLEMENTATION
  - The implementation is done using a type of Neural Network that allows connections only to the output direction, called Feedforward Neural Network.
  - The activation function of the hidden layer is an hyperbolic tangent in a reduced form.

$$Y(x) = 1 - \frac{2}{1 + e^{(2x)}}$$

IMPLEMENTATION of the NEURAL NETWORK

```
/*-------------------------------------------------------------
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  UMa - Universidade da Madeira
  2007/2008
  Versão 1.7
/*-------------------------------------------------------------
#include "xparameters.h"
#include "xuartlite.h"
#include "xstatus.h"*/
#include "datat_neurnet.h"
#include "inputs.h"
#include "math.h"
#include "stdio.h"
#include <sys/types.h>
#include <sys/time.h>

int criaNetwork(NEURAL_NETWORK *network)
{
      network->cria_input  = 0;
      network->cria_neuron = 0;
      network->cria_output = 0;

    CriaListInputs(&network->inputs,b_insert_er
      CriaList_connect(&network->connections,0)
      CriaGrafoNeurons(&network->neurons,b_inse
      return 0;
}

int DeleteNetwork(NEURAL_NETWORK *network)
{
      DeleteListInputs(&network->inputs);
      DeleteList_connect(&network->connections)
      DeleteGrafoNeuron(&network->neurons);
      network->cria_input  = 0;
      network->cria_neuron = 0;
      network->cria_output = 0;
```
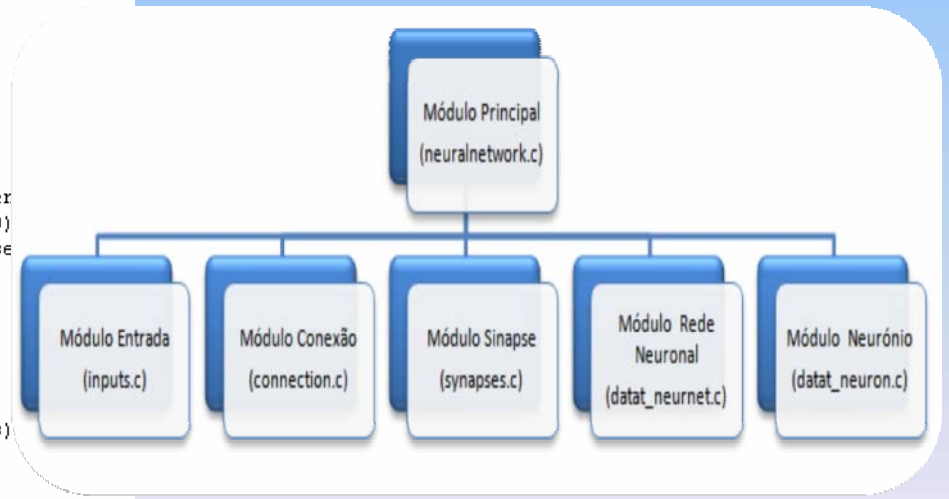

mmed was developed with the generic, i.e., the network would variable number of inputs and

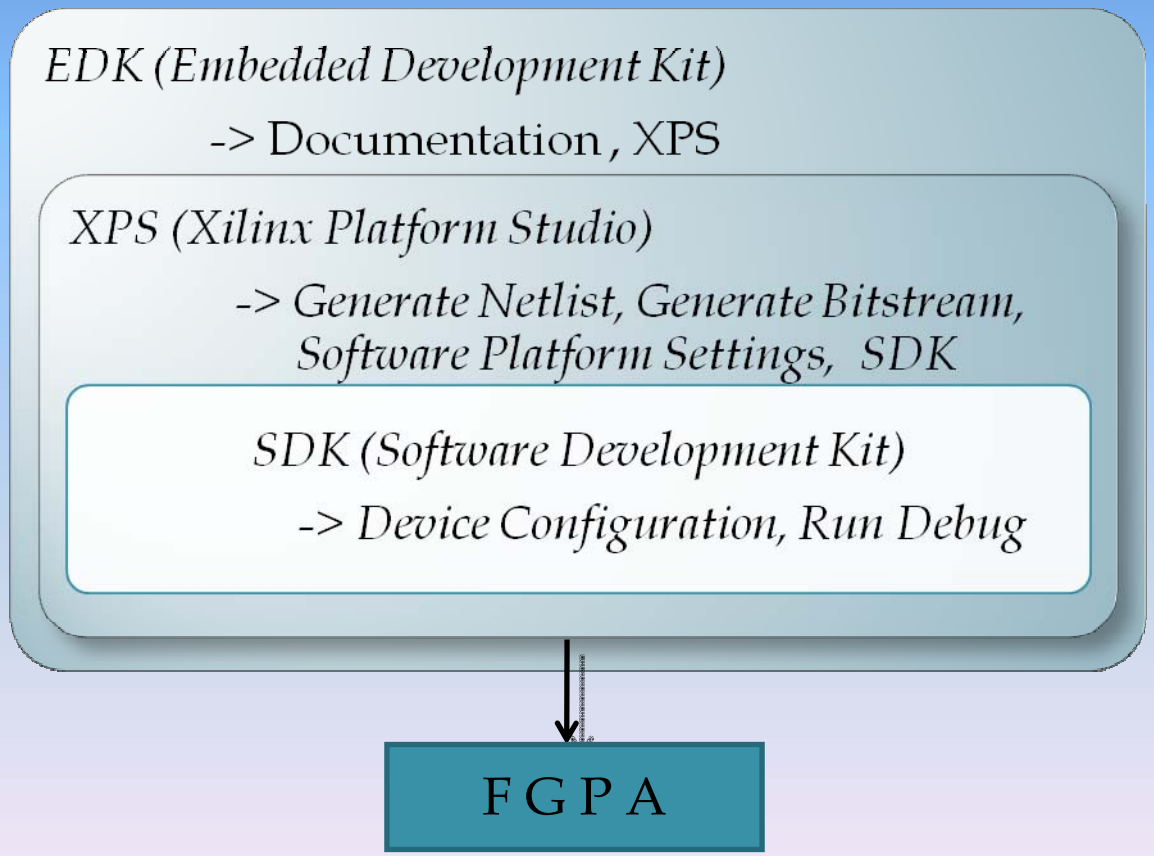


IMPLEMENTATION of the NEURAL NETWORK

- For the internal representation floating-point notation with simple precision was chosen, since this allows the representation of larger numbers with the same number of bits, when compared to fixed point notation.
- To increase the processing speed of the hardware implementation, a Floating Point Unit was added to the configuration of the MicroBlaze embedded system.

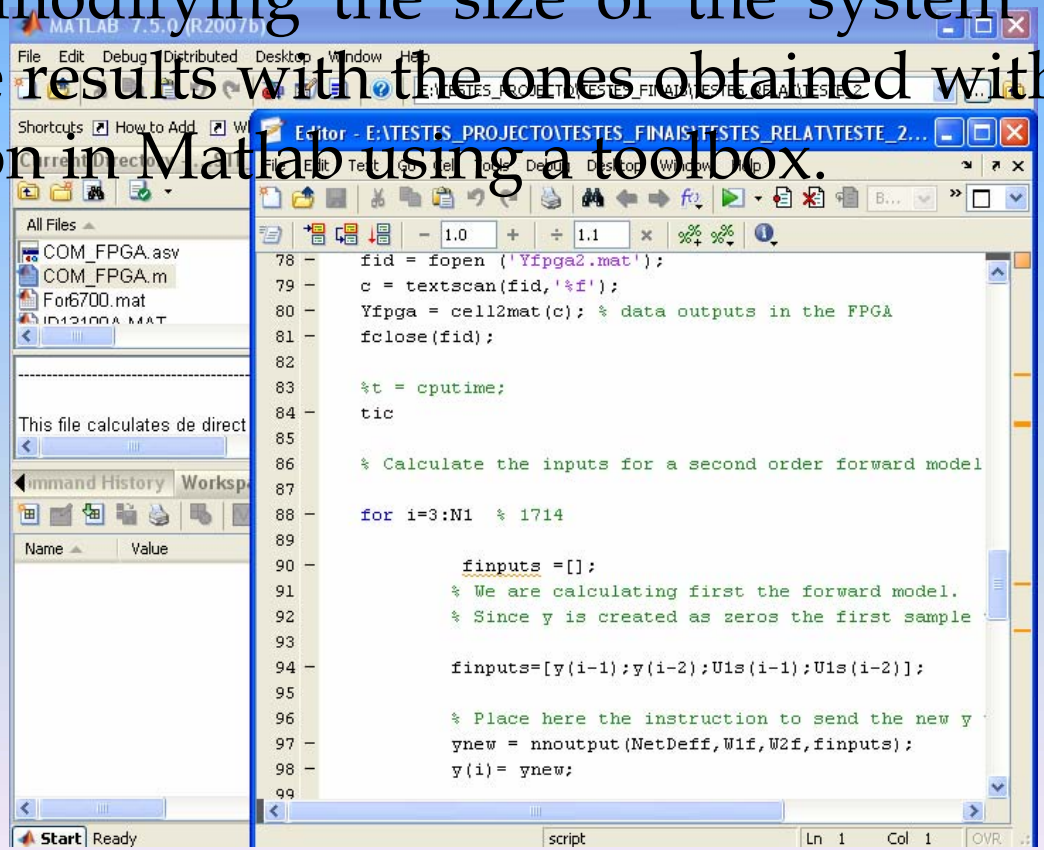
IMPLEMENTATION of the NEURAL NETWORK

Flow of the work with Xilinx's tools



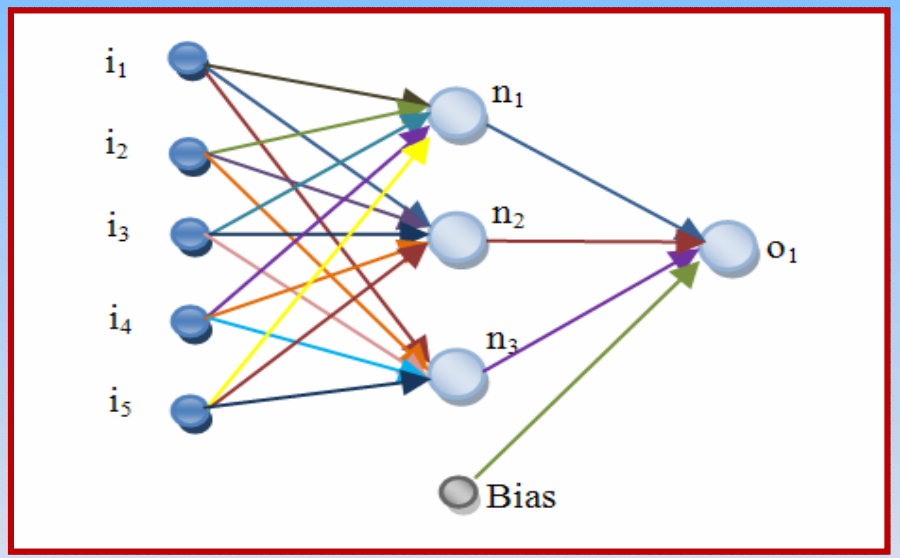
Tests

The tests were used to verify the correct operation of the network, modifying the size of the system and comparing the results with the ones obtained with an implementation in Matlab using a toolbox.



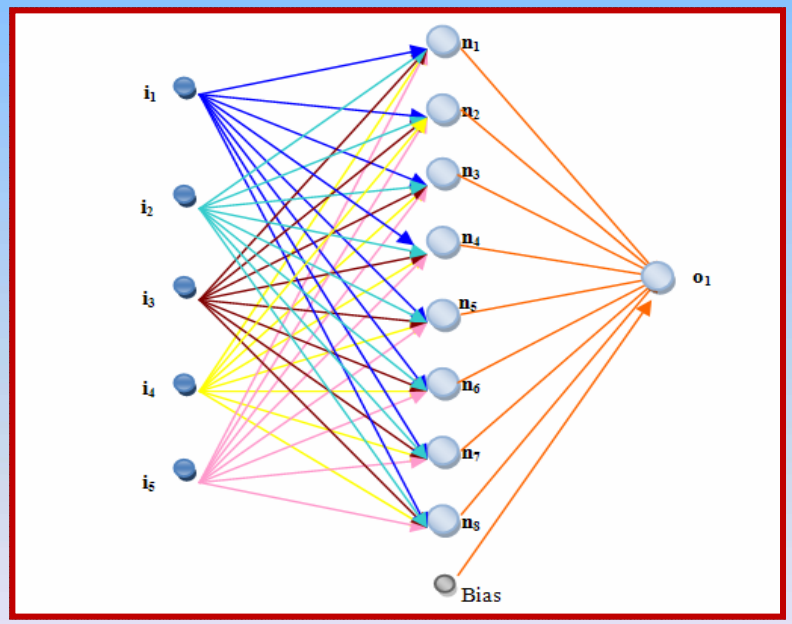
Tests

The structure of the Neural Network model For6700



Tests

The structure of the Neural Network model FORGA001



Tests

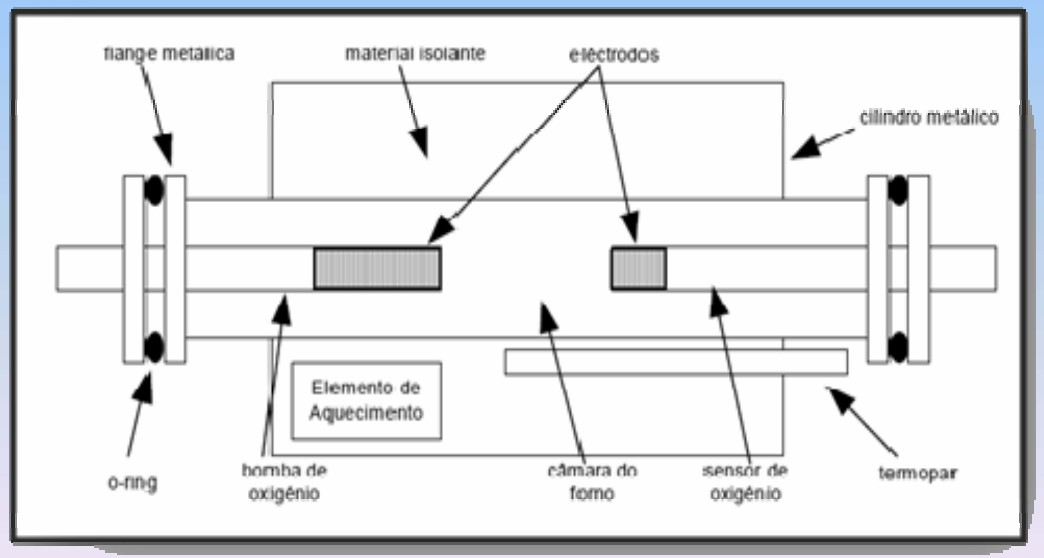
After verifying the good operation of the network and test some different network sizes, the implemented solution was submitted to a comparison with an application developed in Matlab.

Tests

All tests carried through in Matlab were done using data from a real system.

This system is an electric kiln.

Schematic view of the kiln



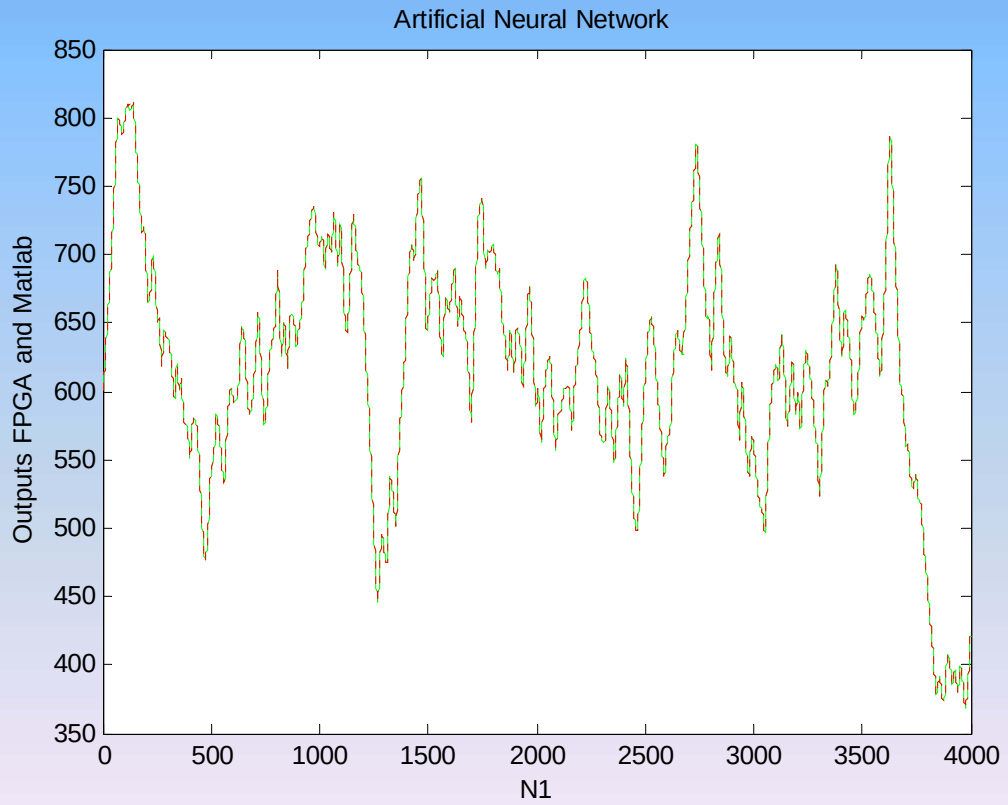
Tests

The electric kiln that was built as part of a research project and had the objective of developing a kiln with high degree of control of the profiles temperature profiles for the ceramic and glass industry.

The area of intended operation was around 750° C, there is an upper limit of 1200° C.

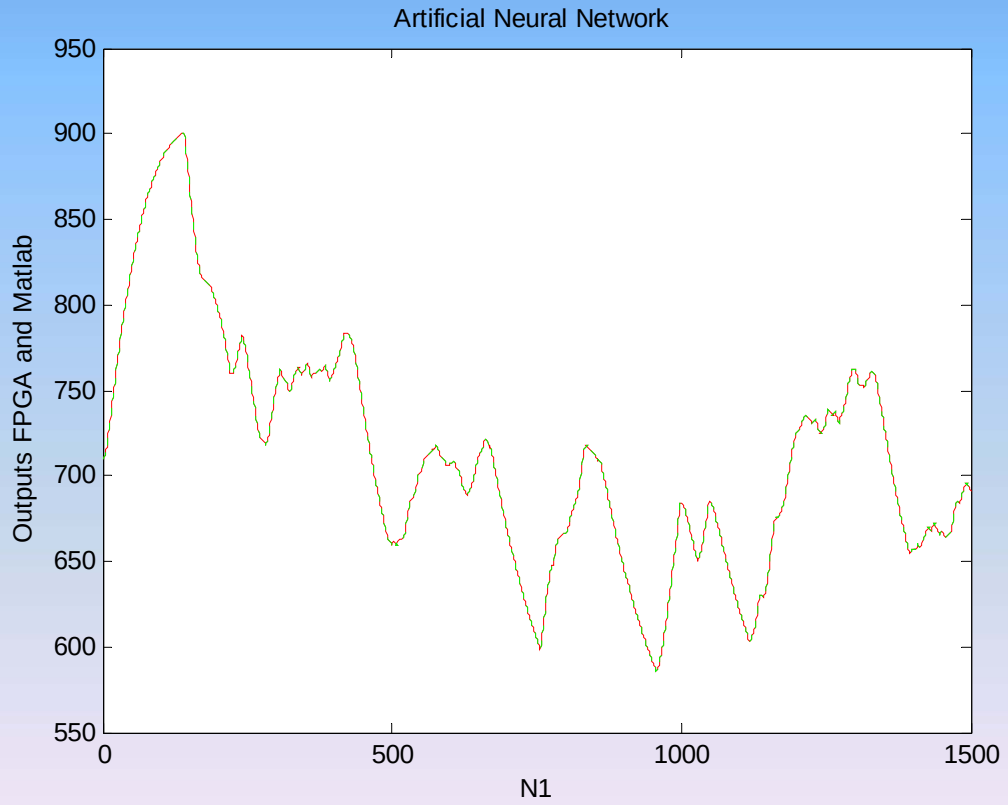
RESULTS

- Output obtained for reference ID050300 with model For6700



RESULTS

- Output obtained for reference ID13100A with model For6700



RESULTS

Mean Square Error

Neural Network	Implementation Matlab / FPGA		
	ID050300	ID13100A	DT030103

	ID050300	ID13100A	DT030103
For6700	$8{,}3660 \times 10^{-20}$	$8{,}5372 \times 10^{-20}$	$8{,}1097 \times 10^{-20}$
FORGA001	$8{,}4874 \times 10^{-20}$	$8{,}7831 \times 10^{-20}$	$8{,}4063 \times 10^{-20}$

RESULTS

- The analysis of the values allows us to conclude that the precision obtained in the FPGA implementation with the embedded MicroBlaze, is very good.

RESULTS

In the hardware the time necessary from processing each of the tests was registered:

- 1434ms, 2147ms and over 42s

  In this last test an overflow occurred, since the microprocessor was running at 100MHz and has 32 bits we can be sure the test took more than 42s.

In Matlab, using a 2.8GHz processor, the time was registered:

- 62ms, 109ms and 283ms.

CONCLUSION

- This work allowed verifying important aspects regarding the hardware/software implementation, including the flexibility and the time of development of project.

- The great potentiality of the hardware chosen for the implementation was also verified, observing that, after all the network configuration, we used only 33% of the resources offered by the FPGA.

CONCLUSION

- The tests made it possible to verify the performance of the network and allowed us to reach the conclusion the implementation is accurate.

- Although this implementation is slower than the one made using a PC, a FPGA board is less expensive than a PC.

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THANK YOU !

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