

Transceiver Design Basics

Renesas Technology Europe

Systems Platform

Dr. Mirco Pieper

13/10/2009

Overview

- Communication chain
- Main implementation parts of TX and RX
- Details for embedded modem implementation
- The new RX microcontroller

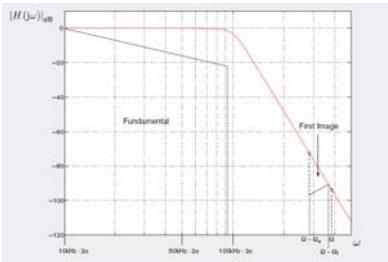
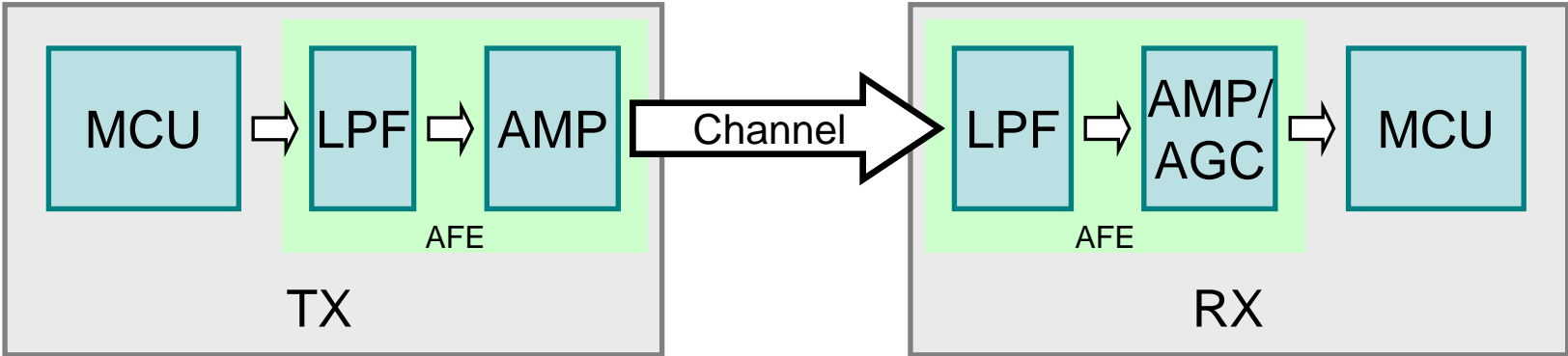
Communication chain

TX

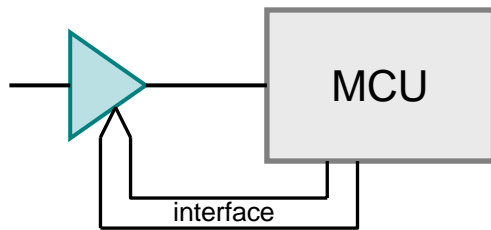
- Data source / data modulator (MCU)
- Low pass filter for image removal
- Transmission amplifier

RX

- Anti aliasing filter
- Automatic gain control
- Data demodulator (MCU)

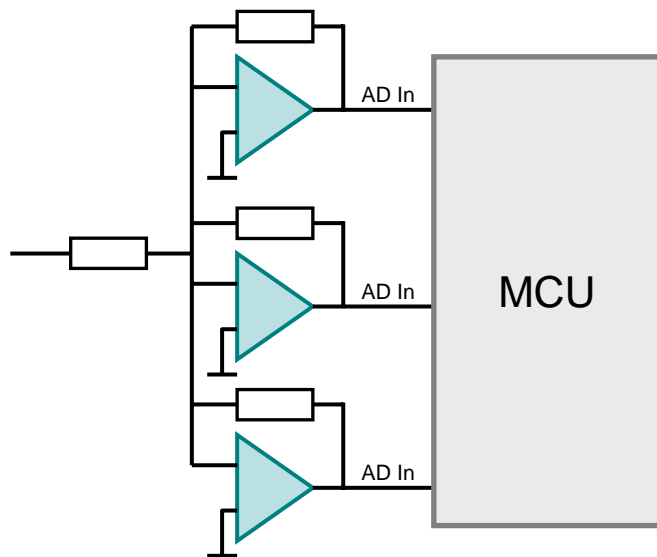


Automatic Gain Control solutions



High performance AGC

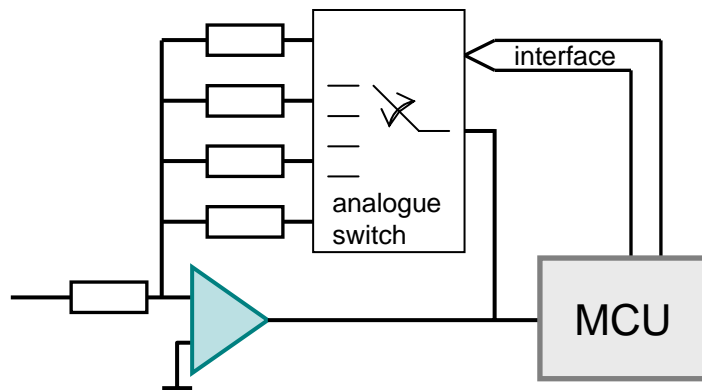
- Variable gain amplifier (VGA) needed
- Gain range depends on VGA (linear)
- Digital interface or DAC needed to control VGA



Discrete AGC

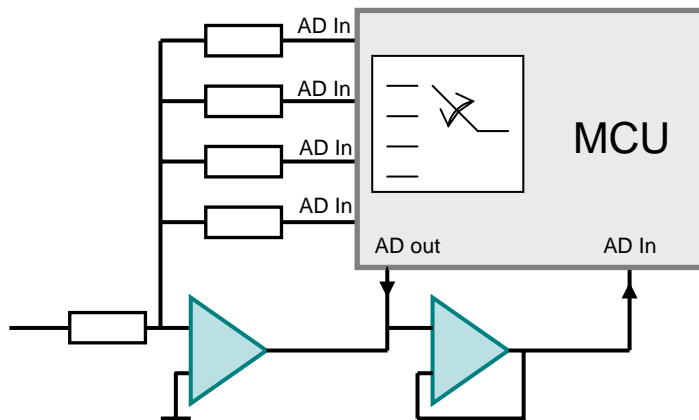
- Each gain stage requires Op Amp
- General purpose Op Amp
- MCU must have several ADC inputs

Automatic Gain Control solutions



Analogue switch based discrete AGC

- Analogue switch needed
- Digital interface to control switch needed
- Number of gain stages depend on analogue switch
- Only one Op amp needed
- Only one ADC input needed

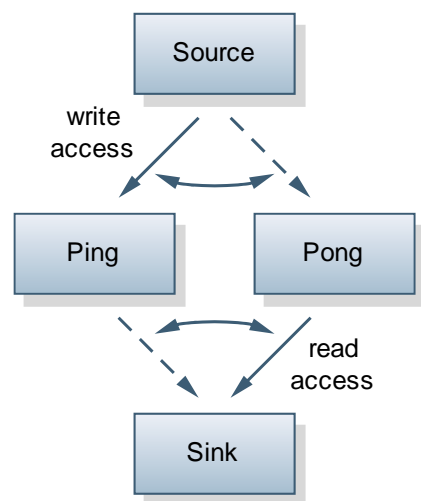


Discrete AGC

- Same performance as above
- No analogue switch needed
- No interface needed
- Number of gain stages depend on ADC inputs

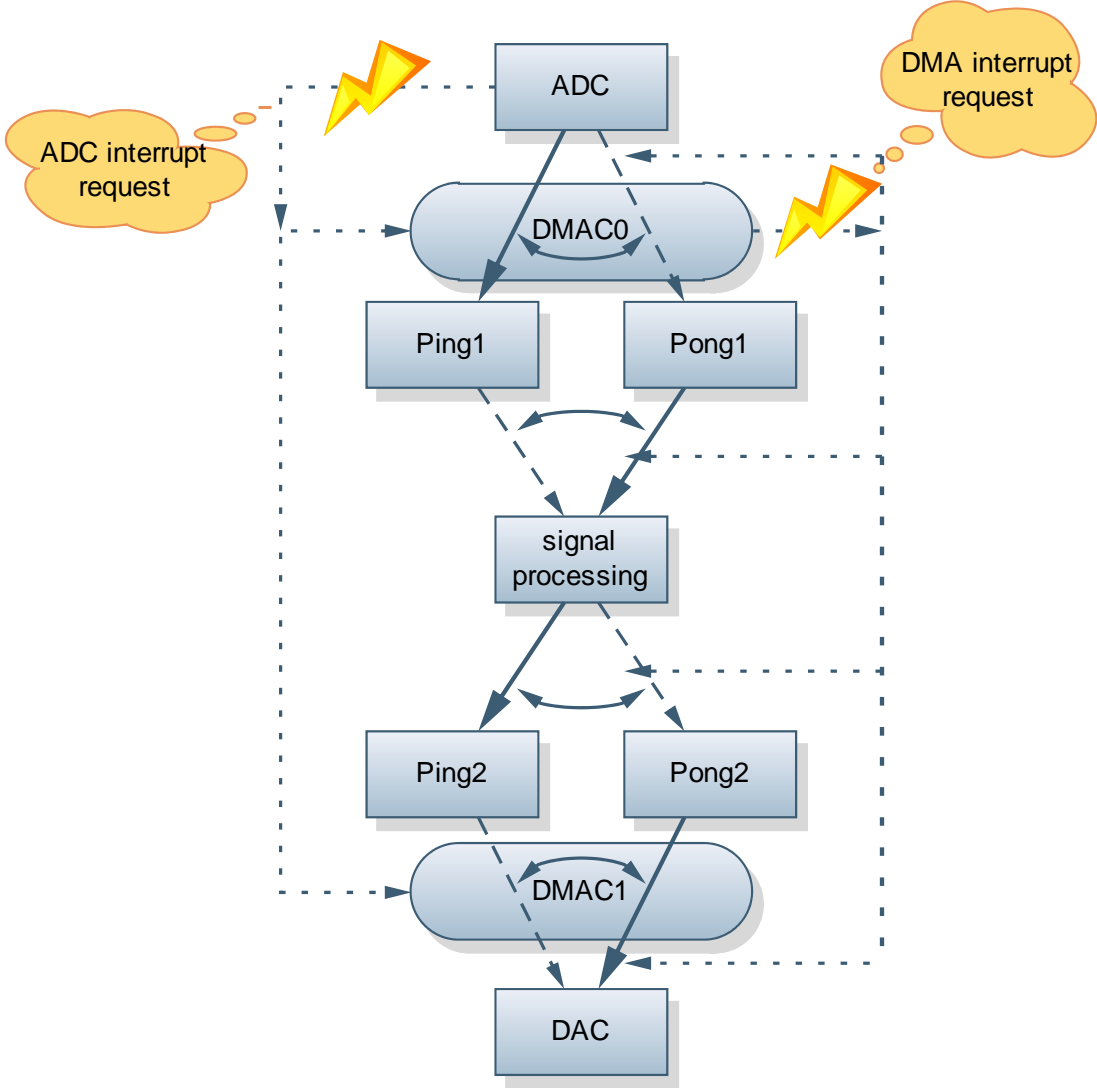
Data capturing

- Incoming data must be capturing while previous data are processed!
- DMA based Ping-Pong buffer
- Data are written to the Ping-buffer while data are read from the Pong buffer
- Pong-buffer has to be processed before Ping-buffer is full
- After Ping-buffer is full switch buffer pointers
- Incoming data rate and buffer size define the available processing time



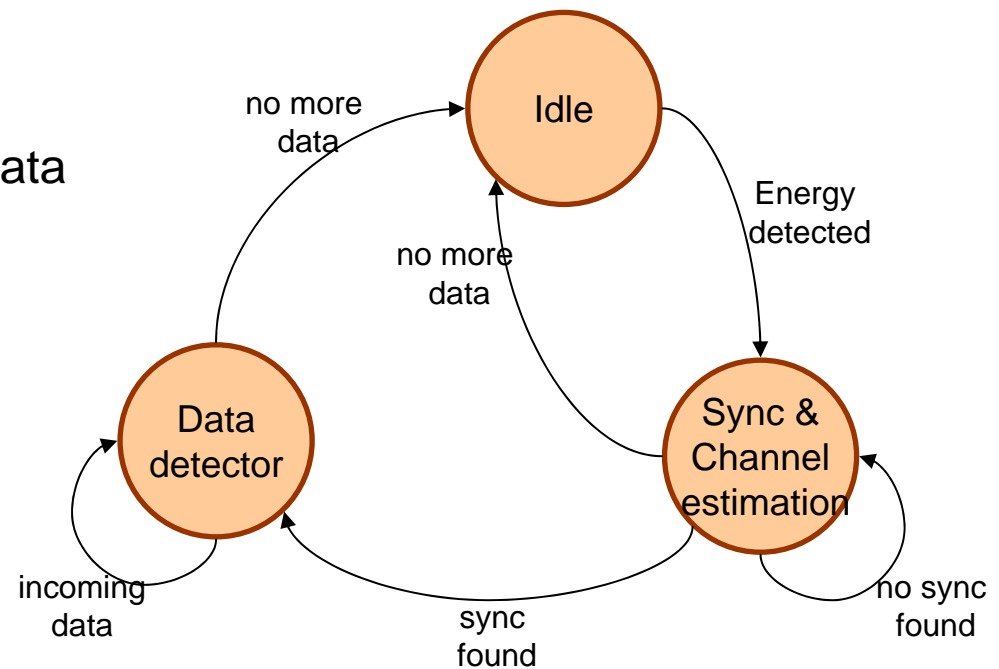
100 byte @
400 kbps
=> 2 ms
processing
time

General signal processing overview



RX state machine

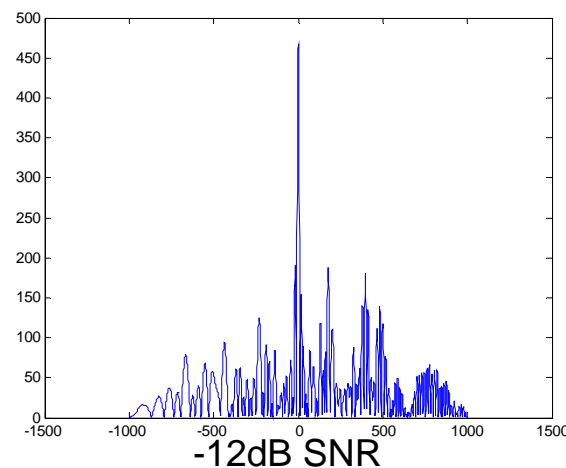
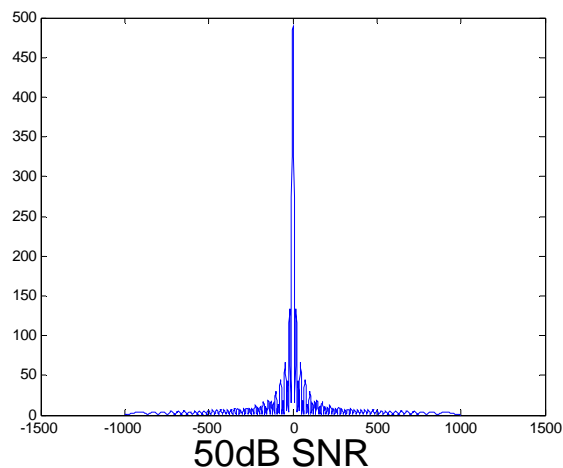
- Wait for signal
 - Energy detection
 - Envelope detection
- Preamble detection
 - Channel estimation
 - Synchronization
 - Calculate starting point of data
- Data demodulation



What is needed to receive a frame?

- How to detect a frame?
- How to compensate channel impact?
- How to set up automatic gain control section?

- Add a preamble (excellent aperiodic autocorrelation properties) to detect a frame in noise environment!
- Use preamble or additional training section for channel equalization



FFT analysis

- Radix-2
- Radix-4
- Split Radix FFT (SRFFT)
- Fast Hartley Transform (FHT)
- Quick Fourier Transform (QFT)
- Decimation-in-Time-Frequency (DITF)

Mathematical operations involved in a 1024-point complex FFT

Algorithm	Float Mults	Float Adds	Int Mults	Int Adds	Bin Shifts
Radix-2	20480	30720	0	15357	1024
Radix-4	15701	28842	336	8877	2738
SRFFT	10016	25488	502	12448	2937
FHT	18704	32056	0	8367	4246
QFT	8448	31492	16	70058	316
DITF	16640	28800	1076	18839	1086

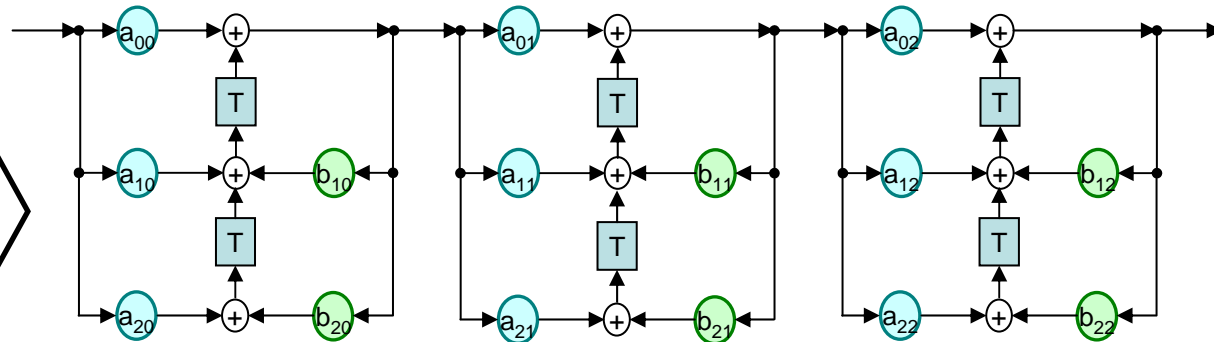
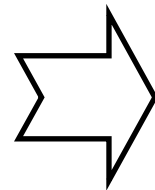
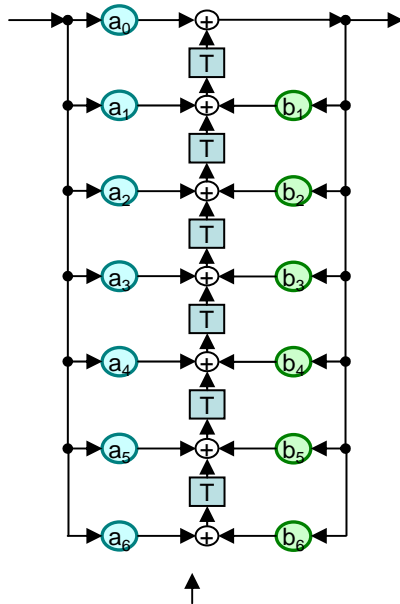
Number of operations is equivalent to speed on CISC architecture

Fastest implementation on RISC architectures due to pipelining and cache usage

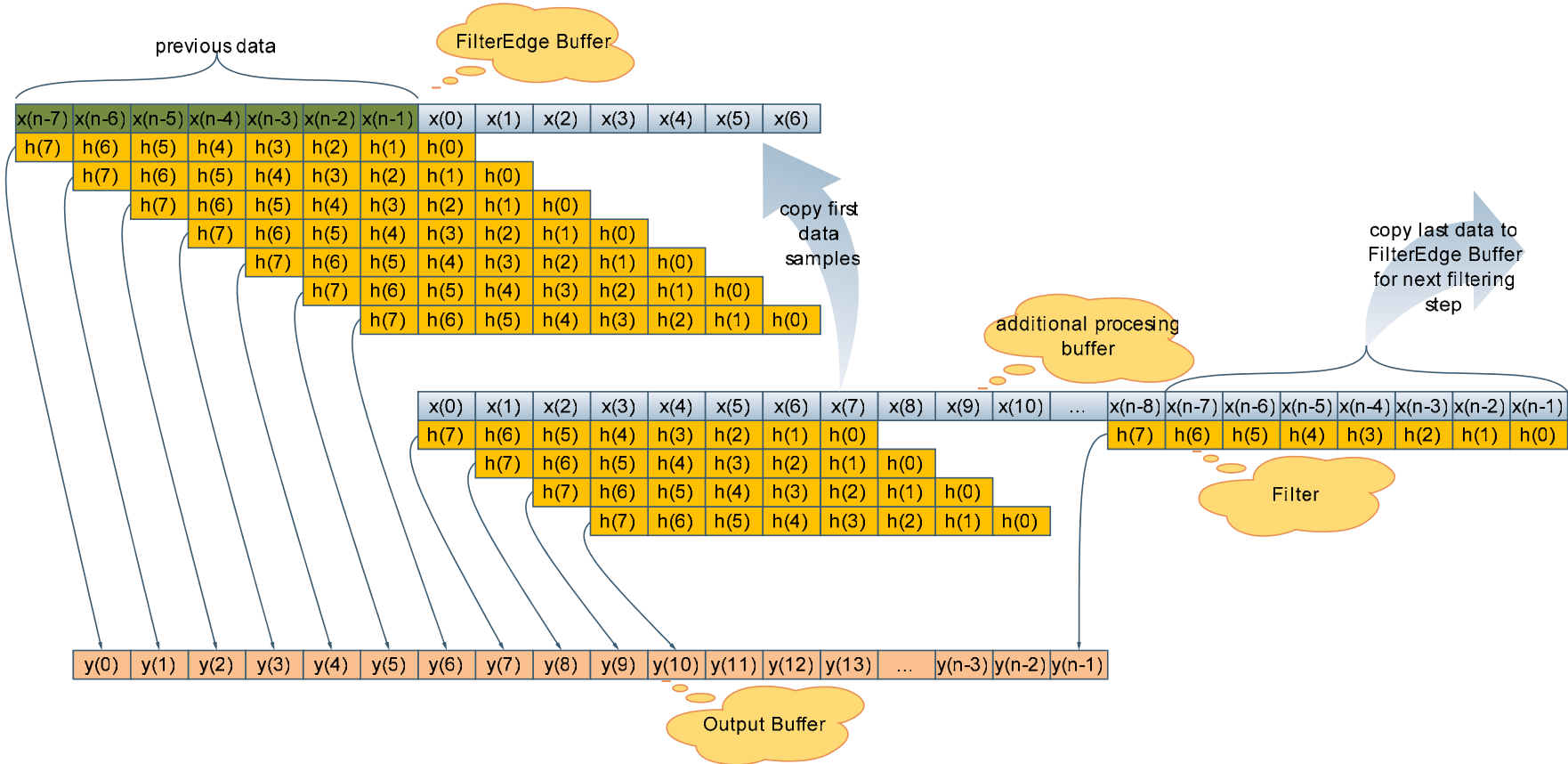
Second Order Structure-Filter

- Convert an IIR Filter to cascaded IIR filters of lower order (2nd order)
- Filter is stable if each sub-filter is stable
- Less quantization error impact of filter coefficients

$$H(z) = \frac{\sum_{n=0}^6 a_n \cdot z^{-n}}{1 - \sum_{n=1}^5 b_n z^{-n}} \quad \Rightarrow \quad H(z) = \frac{\sum_{n=0}^2 a_{n0} \cdot z^{-n}}{1 - \sum_{n=1}^2 b_{n0} \cdot z^{-n}} \cdot \frac{\sum_{n=0}^2 a_{n1} \cdot z^{-n}}{1 - \sum_{n=1}^2 b_{n1} \cdot z^{-n}} \cdot \frac{\sum_{n=0}^2 a_{n2} \cdot z^{-n}}{1 - \sum_{n=1}^2 b_{n2} \cdot z^{-n}}$$



Sliding window based filtering

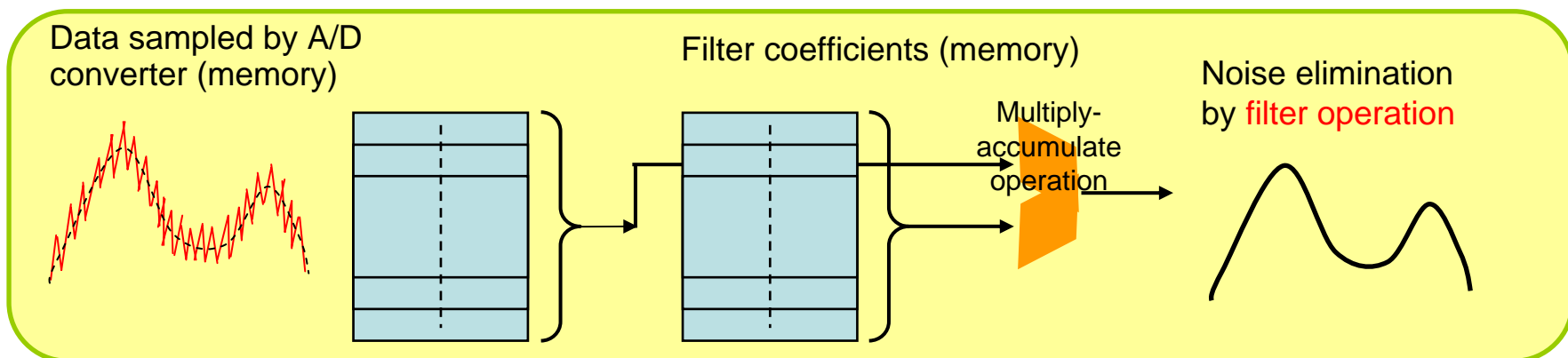
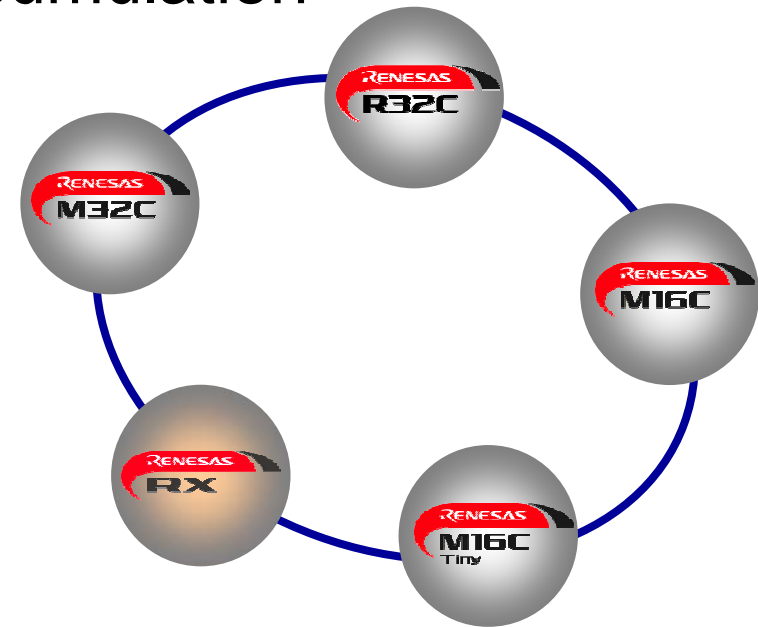


RMPA - Repeat Multiply and Accumulation

- Performs sum-of-product operation, with the
 - multiplicand address indicated by A0,
 - the multiplier address indicated by A1, and
 - the number of operation indicated by R7R5.
 - The result is stored to R3R1:R2R0 as 64-bit data.

- Cycles of word based RMPA
 - R32C: $11 + 1.5m^*$ cycles
 - M32C: $7 + 2m^*$ cycles
 - M16C80: $7 + 2m^*$ cycles
 - M16C: $6 + 9m^*$
 - M16C Tiny: $6 + 9m^*$

*m is the number of operations



Fast Convolution – Frequency domain vs. Time domain

Comparison of 32nd order FIR-filtering based on convolution and FFT.

M = 960 data
L = 32 FIR filter
B = 480 input buffer
N = 512-Point FFT

Frequency domain

■ 960 input values must lead to 991 output values

■ 512 point FFT (zero padding)

■ FFT => $(N) \log_2 (N)$ operation
=> $4608 * 2 = 9216$ operations

■ Required operations

■ FFT (9216)

■ Filter tabs are pre calculated

■ 1024 mults

■ IFFT (9216)

■ 32 additions

⇒ $9216 + 1024 + 9216 + 32 =$
19488 operations

Time domain

■ Required operations

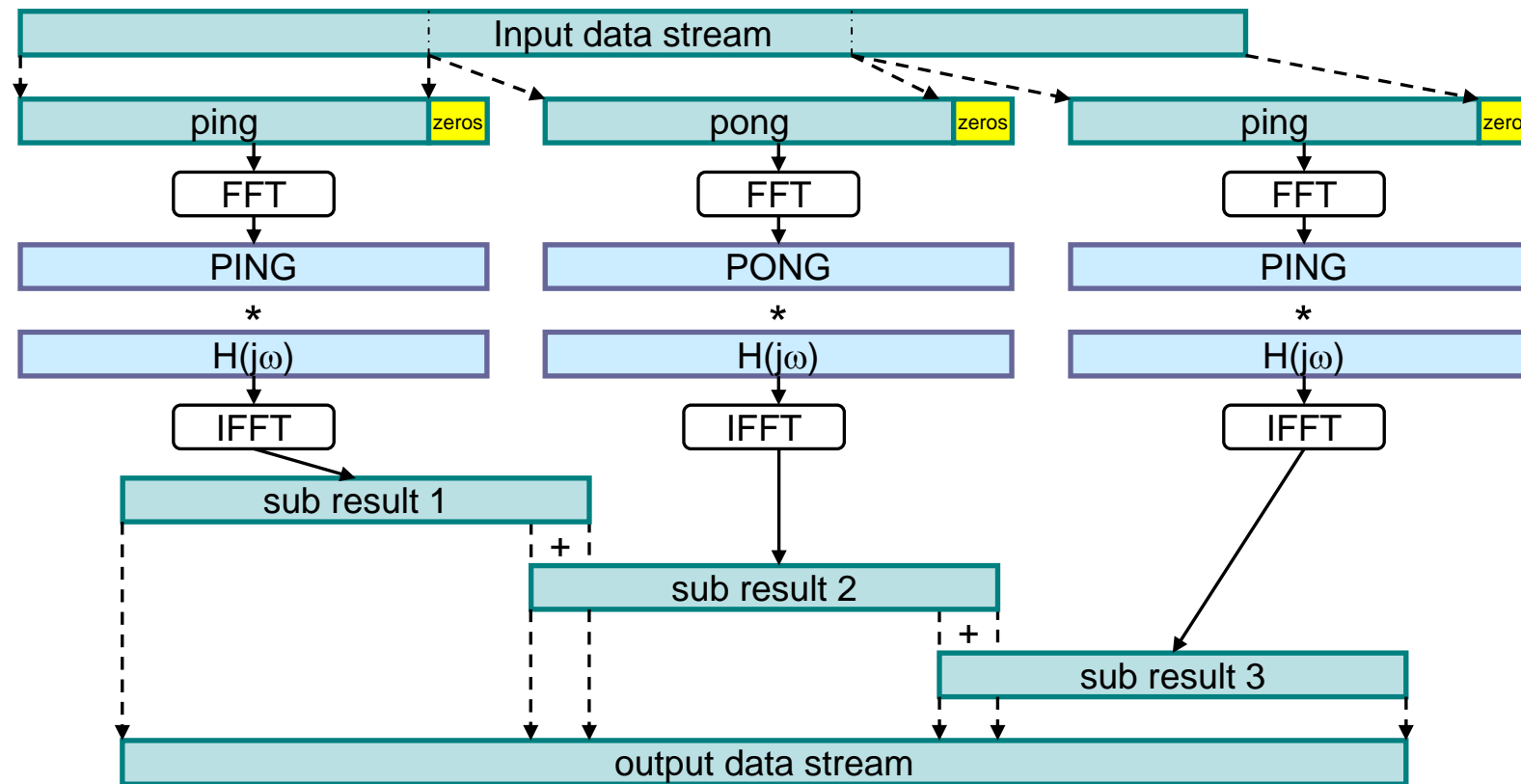
■ $960 * 32$ mults

■ $960 + 32 + 1$ additions

⇒ $30720 + 960 + 32 + 1 =$
31713 operations

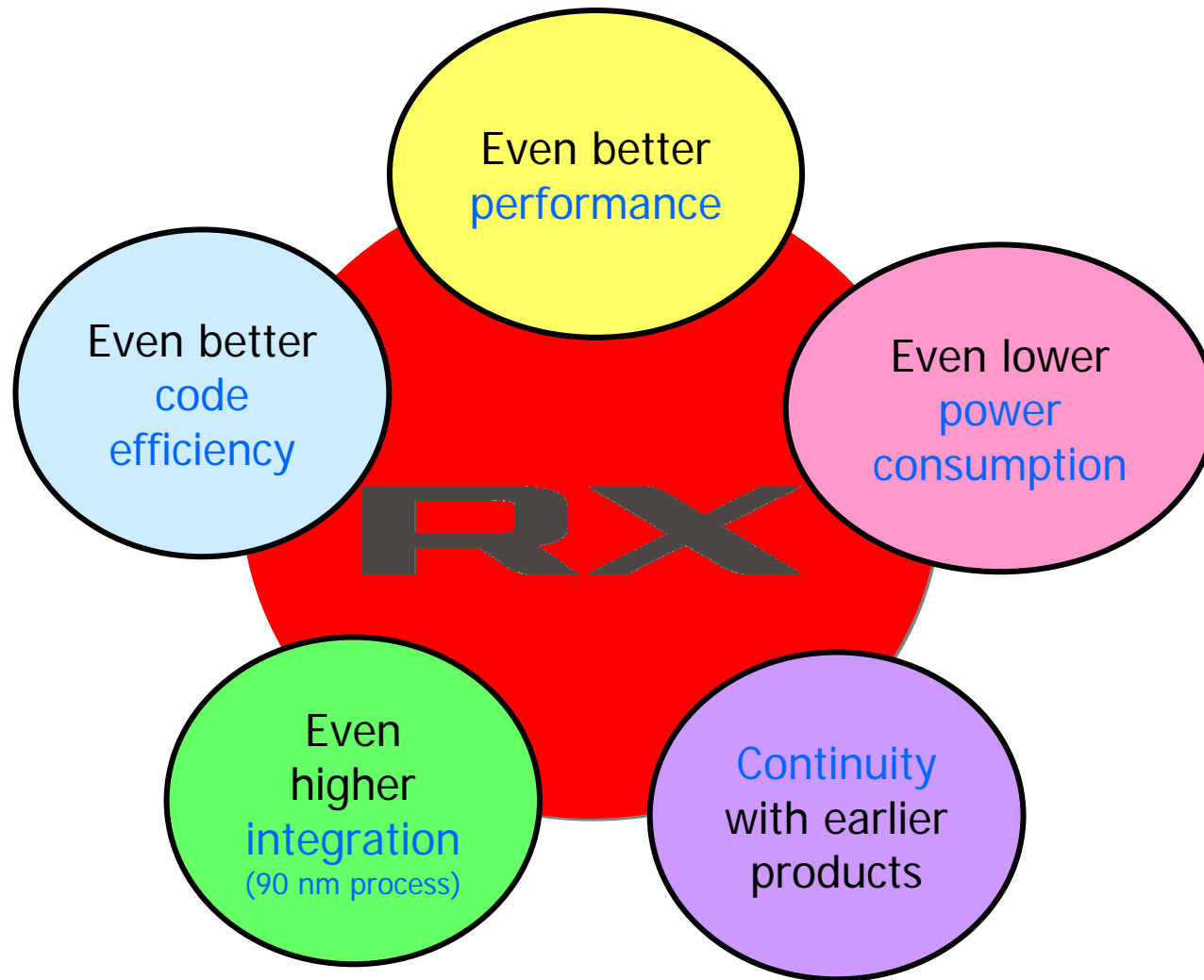
Overlap and Add Method

- Continuous data stream is split into segments due to ping pong buffering
- Signal processing of first and last part of buffer is related data of previous and following buffer
- Overlap and Add method to combine adjacent data



The RX Concept

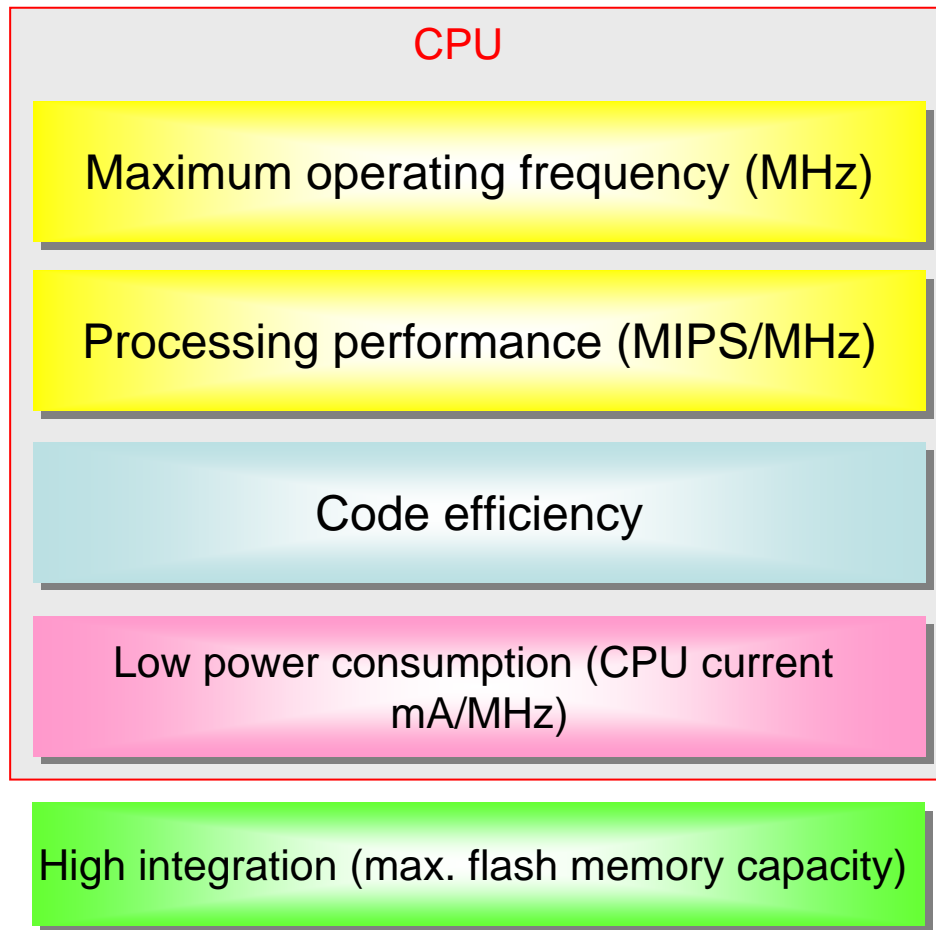
- Enhance the current Renesas 16 and 32 bit CISC device families to meet future market requirements



RX Target Indices



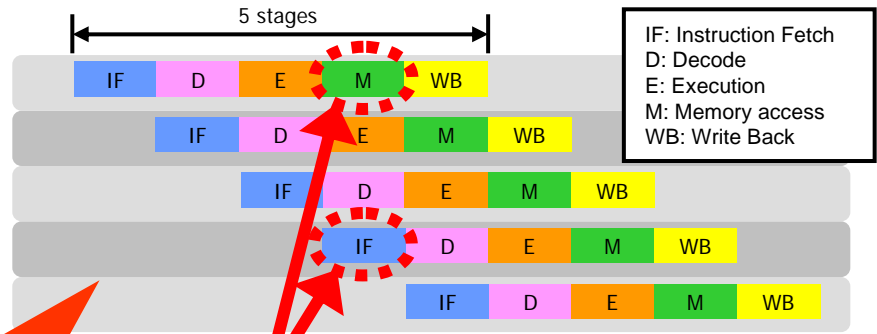
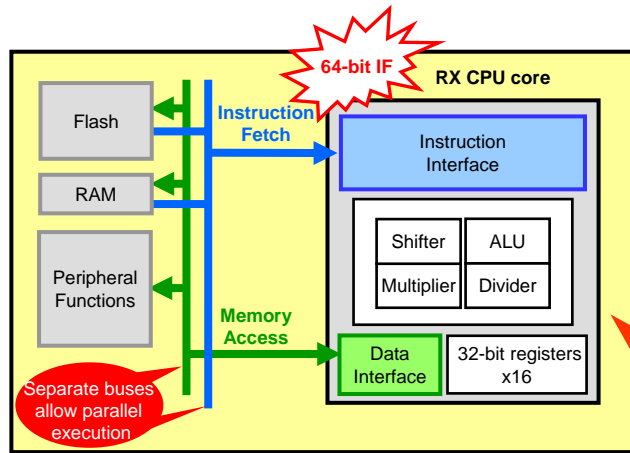
- The aim is to realize higher maximum operating frequency, better performance, improved code efficiency, and lower power consumption than previous products, by enhanced design techniques and utilising 90 nm technology.



Improved basic performance and code efficiency

Comparison with previous products	Design target
5X	200 MHz
2X	1.65 MIPS/MHz
30% improvement	
1/3	0.03 mA/MHz
4x	4 MB

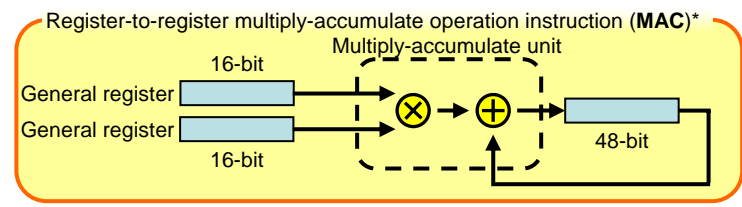
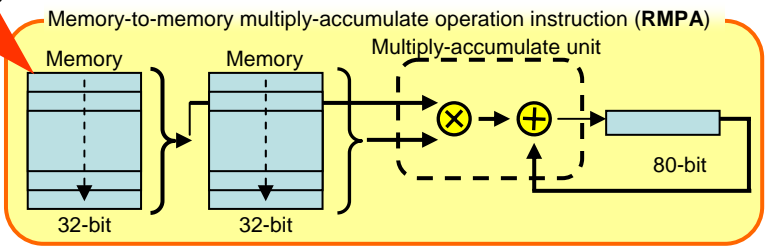
Features of RX CPU – Improved Performance



Harvard architecture allows parallel execution

Harvard 5 stage architec. pipeline
RX
FPU DSP functions

- 32-bit, single precision, IEEE-754
- No load-store operation needed
- 1 clock min, 18 clocks max per operation





Renesas Technology Europe

©2008. Renesas Technology Europe Ltd., All rights reserved.

RX610 Group Specifications

Features: 165MIPS, 50mA and single cycle Flash access at 100MHz operation

10bit ADC 4ch x 4unit

■ High-performance CPU

- High-speed operation: Single-state basic instruction execution: 10ns(100MHz@3.0 to 3.6V)
- 32bit multiplier/divider, multiplier-accumulator and single-precision FPU

■ On-chip memory

- Flash: 2 MB/RAM 128 KB
- Flash: 1.5 MB/RAM 128 KB
- Flash: 1 MB/RAM 128 KB
- Flash: 768 KB/RAM 128 KB
- No flash memory/RAM 128 KB

■ Peripheral functions

- -External bus expansion: 16-bit separate bus (ROM/RAM I/F, byte control SRAM I/F)
- -Transfer module: DMAC and DTC
- -Timers:
 - High-performance general purpose timer: 16 bits x 12ch (TPU)
 - Timer optimized for OS and similar applications: 16 bits x 4ch (CMT)
 - General-purpose timer: 8 bits x 4ch (TMR)
- -High-speed 10-bit A/D converter (conversion time: 1μs)
- -10-bit D/A converter x 2ch
- -Communication functions: Clock synchronous/asynchronous SCI x 7ch I2C x 2ch (Fast-mode Plus)

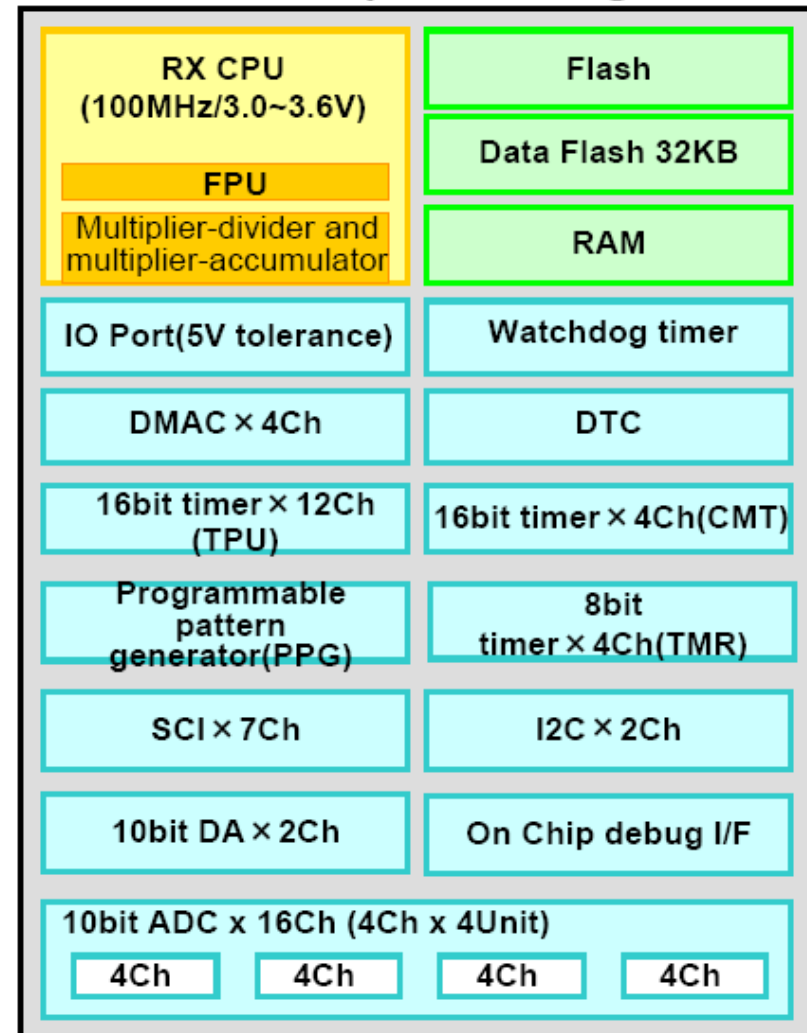
■ Development environment

- On-chip debug emulator
- Full emulator

■ Package

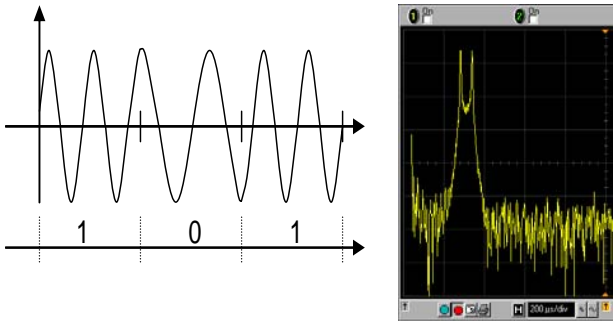
- -LQFP144, BGA176-pin

RX610 Group Block Diagram

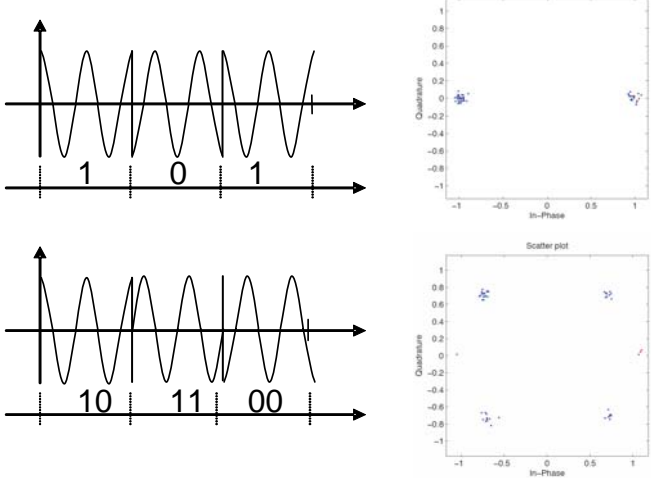


Modulation basics

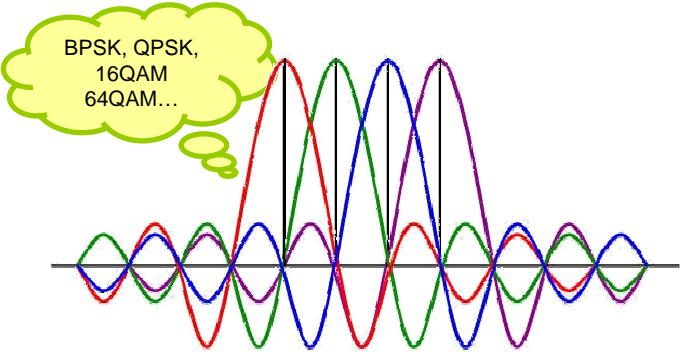
FSK



BPSK / QPSK

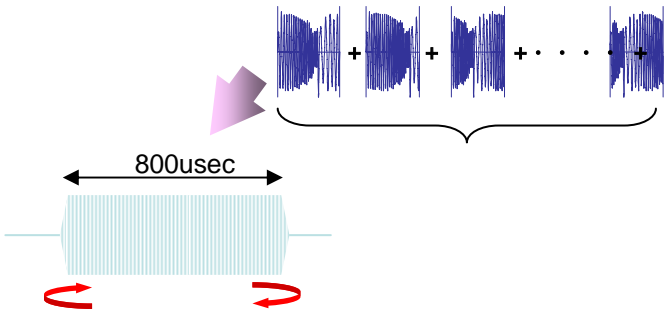


OFDM



DCSK

Connect short waveforms to make long Basic Waveform



Rotate Basic Waveform to make different 64 patterns or 16 patterns waveforms