Implementation performance of an Embedded Architecture for Lab-on-Chip Instrumentation Control and Data Analysis

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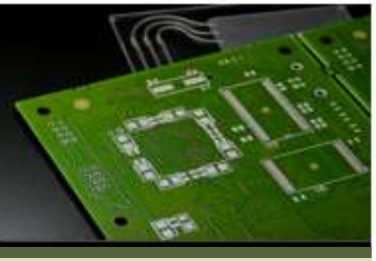
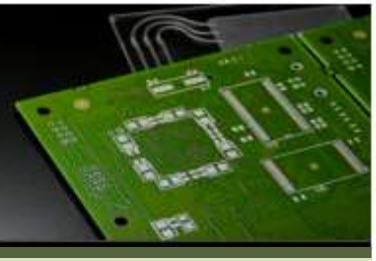


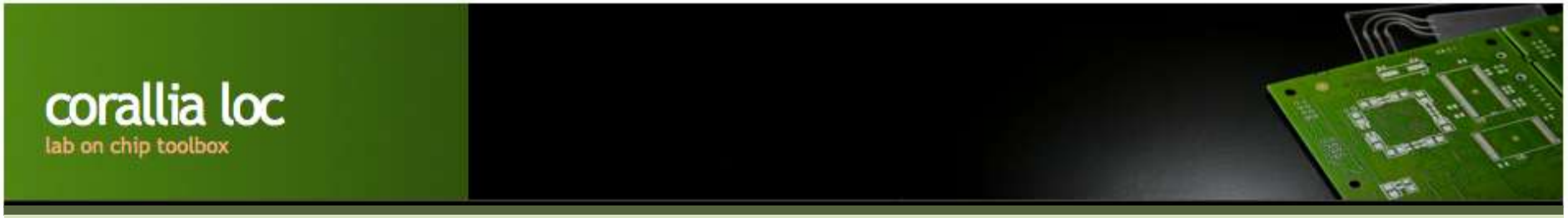
Microfluidics Lab-on-Chip

- Microfluidics-based biochips (Lab-on-Chip, LoC) are DNA or protein microarrays (small or large number of microscopic spots -50 to 200μm diameter-), and a structure of micro-channels and cavities, arranged on a solid surface of a piece of plastic or other neutral material
- On LoCs micro-quantities of biochemical reagents and biological samples are transferred with the “assistance” of micropumps, and microvalves to specially formed cavities (chambers).
- Biochemical reactions in LoCs take place under special conditions (e.g. specific temperature, continuous agitation etc.), so to prepare the sample appropriately and then to electronically detect if there exists a specific Single Nucleotide Polymorphism (SNP) of a gene or a particular antibody that shows the presence of a protein.



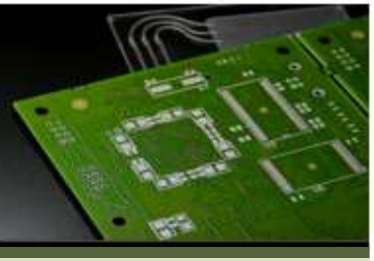
LoC Instrumentation

- LoCs need to be placed in special instrumentation that provide to them all necessary conditions to move appropriately the reagents and samples into their micro-channels, in real time according to the execution of a specific biological protocol, and then to detect if the expected reactions were realised or not.
- First challenge is to accommodate the control needs for valves, pumps, mixers, heaters etc. of the LoCs that are used to prepare the sample and perform the biochemical reaction.
- Then the other challenge is to detect if there was performed hybridisation (successful biochemical reaction), on every single spot of the microarray so to conclude about the existence of specific SNPS of genes and/or proteins.



Corallia Project

- Corallia is a Greek National research project for the Design-Development and pilot application of advanced IP blocks of integrated circuits and sensors for LoC instrumentation and also for subsystems of Molecular Diagnostics for control and measurements of Genetic and other applications that use LoCs (e.g. Point of Care –PoCs-)
- IPs will be building blocks for the development of innovative systems with :
  - Higher precision
  - Significantly reduced size
  - Significantly reduced cost in comparison with the existing today



Corallia Project (2)

- Into Corallia project there will be designed and prototyped :
  - § Biosensors arrays for hybridisation detection
  - § Analogue-Digital integrated circuit for readout of the biosensor array
  - § Digital recovery, processing and machine vision SoC ASIC for the real time optical control of microfluidics (reagents moving into channels, volume estimation, quality control)
  - § Analogue Digital ASIC for the control and driving and monitoring of LoC operation
  - § Integration of the above in a prototype system with the appropriate firmware and software for the user interface

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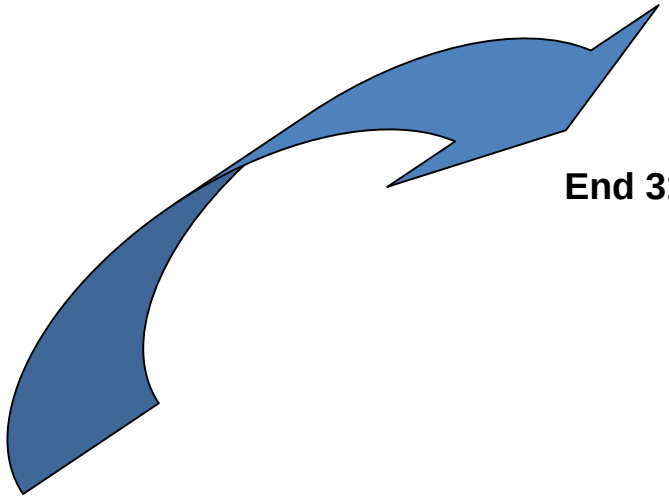
Corallia Project (3)



End 31/01/2013

Start 01/11/2009

Total Budget 3.099.556,66€
773,83 personmonths

Total Funding 2.567.556,50€

TEI Funding 277.200,00€

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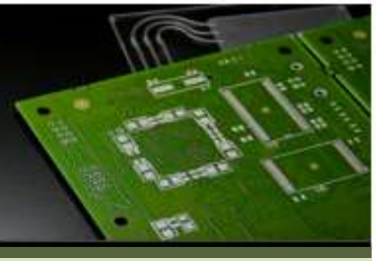
Corallia Project (4)

ACADEMIC PARTNERS

- Technological Educational Institute of Crete
- Institute of Microelectronics DEMOKRITOS
- Electronics Lab University of Thessaloniki
- National Technical University
- University of Patras

INDUSTRIAL PARTNERS

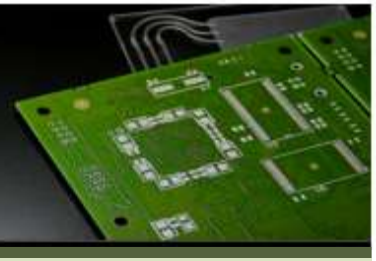
- Micro2Gen Ltd.
- INTRACOM S.A.
- Raymetrics S.A.
- 4Plus S.A.
- Alma Technologies S.A.



Corallia Project (5)

INDUSTRIAL PARTNERS ROLES

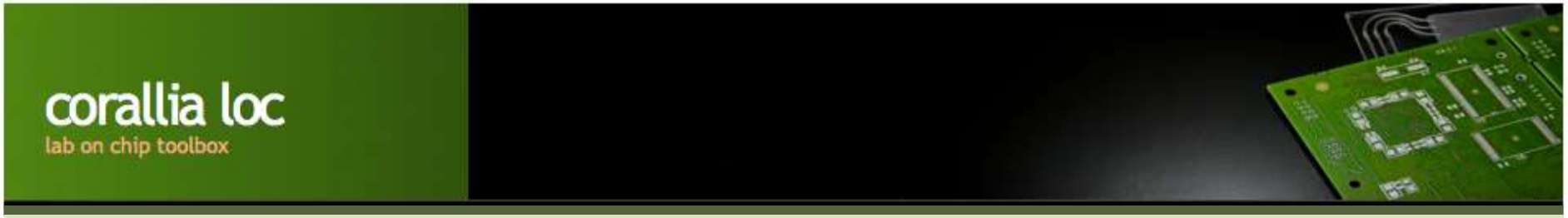
- Micro2Gen Ltd.
  - Specification and Development of a Point of Care System
- INTRACOM S.A.
  - Machine Vision IP Development
- Raymetrics S.A.
  - LoC use in Environmental Applications
- 4Plus S.A.
  - Development of Driving elements for the instrument
- Alma Technologies S.A.
  - Image Compression IP Development



Corallia Project (6)

ACADEMIC PARTNERS ROLES

- Technological Educational Institute of Crete
  - § Integration of the IPs to be developed, Prototype Development and testing
- Institute of Microelectronics DEMOKRITOS
  - § Capacitive Biosensors Development and microfluidics LoC Prototyping
- Electronics Lab University of Thessaloniki
  - § Machine Vision IP Development
- National Technical University
  - § Fictionalization of Biosensors and User Interface Software Development
- University of Patras
  - § Capacitive Sensors Readout Development



Corallia Project (7)

Technological Educational Institute of Crete Role Details

- Workpackage 2 Analogue Digital subsystem for control and machine vision
  - Subsystems Specifications
  - Machine Vision IP Design
  - Firmware Development for the Embedded Processor
  - Machine Vision IP Testing
  - Software Development for the user Interface
- Workpackage 4 : Integration and Prototype Implementation
  - Integration of the control and machine vision subsystem
  - Biosensors control integration
  - Point of Care system testing

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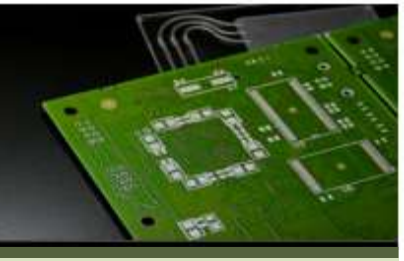

SoC FPGA for the real time optical control of microfluidics

- It is presented here an embedded architecture for accelerating the execution of many machine vision image processing algorithms :
  - § control and moving of the reagents in the LoC by following the edges of the reagents into the micro-channels
    - Microfluidic chip/frame detection
    - Flow fronts and movement detection
    - Microfluidic channel metrics calculation
      - Volume size
      - Velocity
      - Direction
  - § Image compression and frame grabbing for the remote control and monitoring of the LoC
  - § Analogue & Digital Control System for the control of the valves, pumps, mixers, heaters etc.
  - § Future enhancement of the SoC it will be the processing of the images of the hybridised spots that detected fluorescent based targets.

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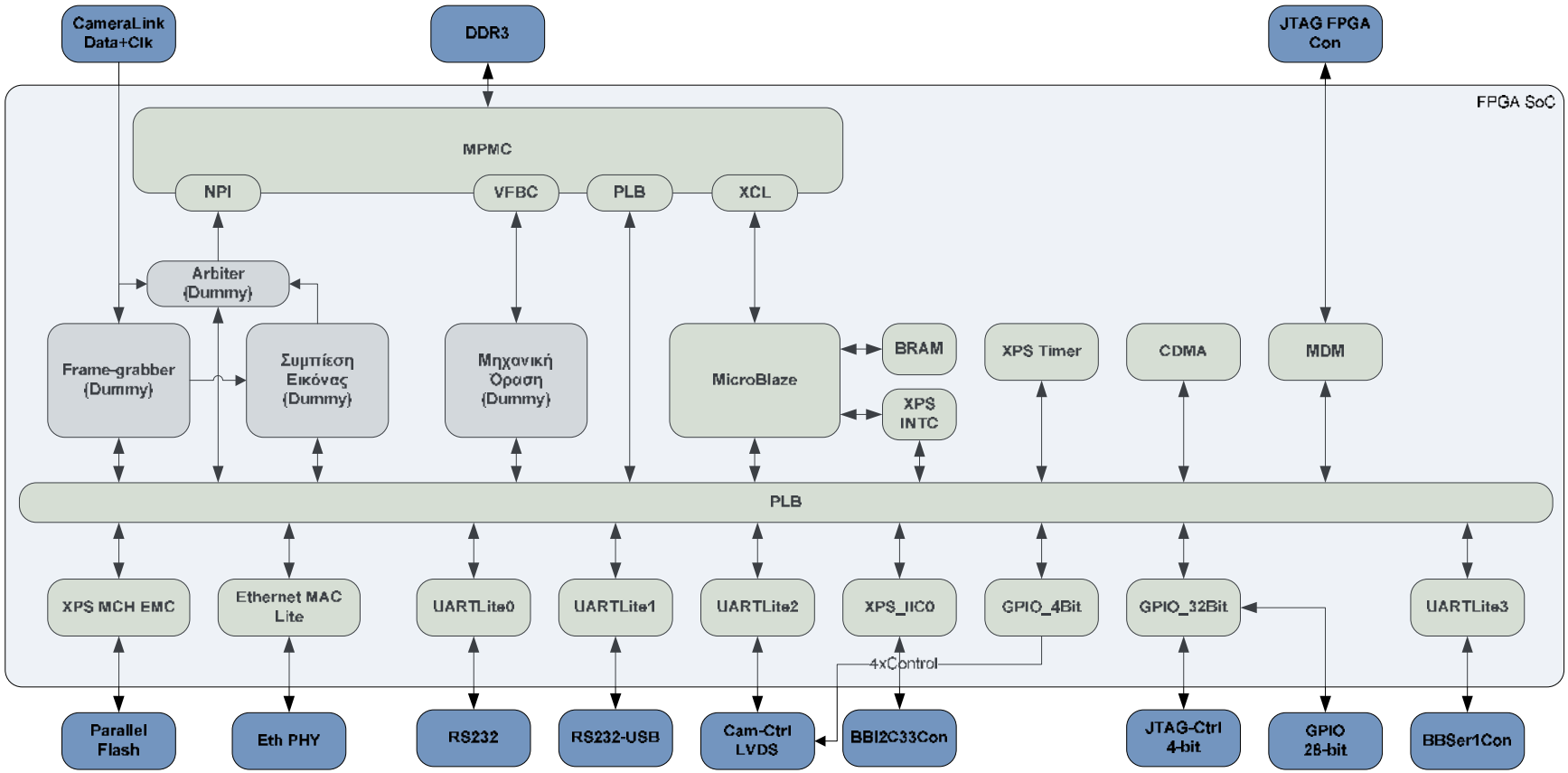
Block Diagram



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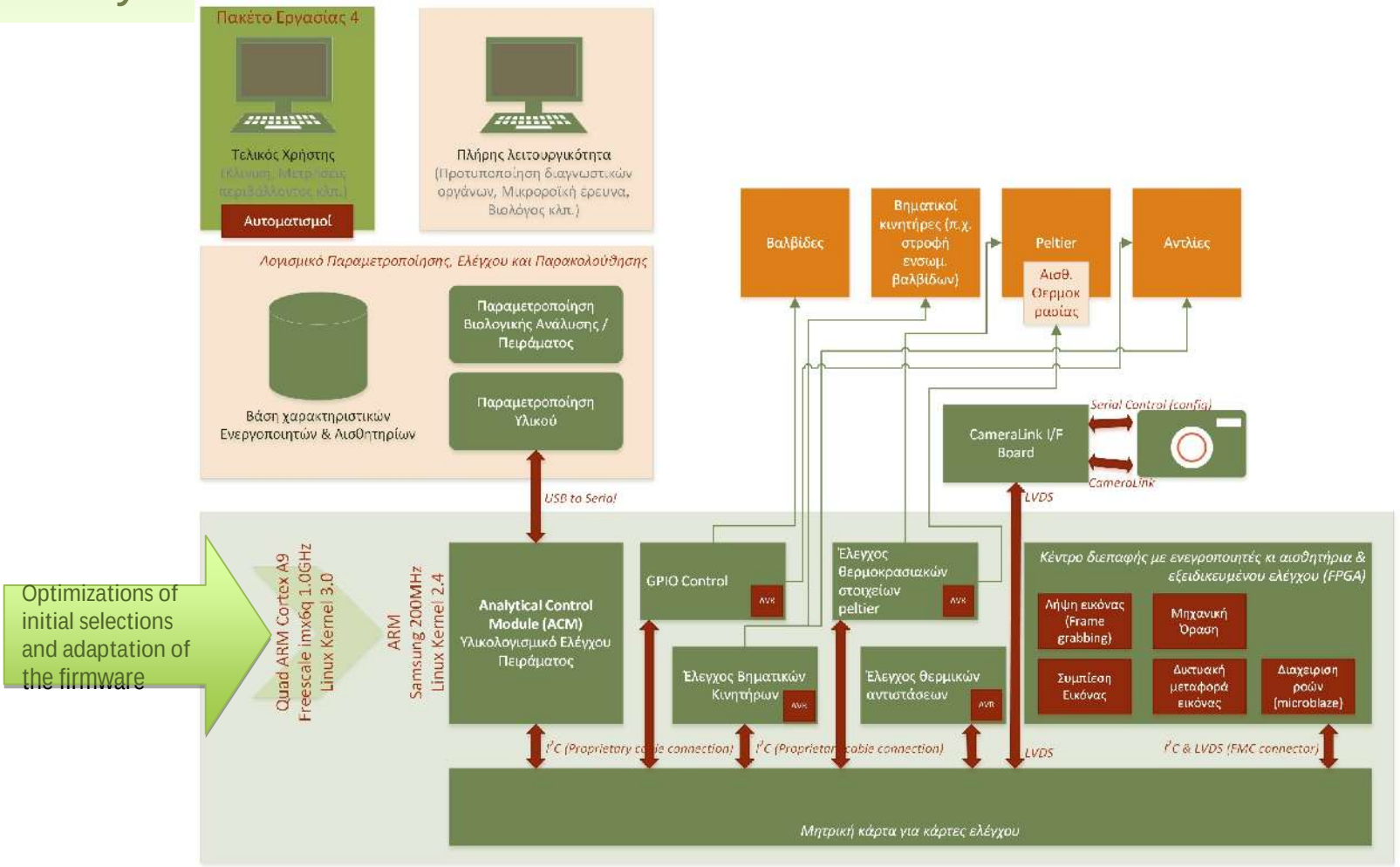
General system architecture



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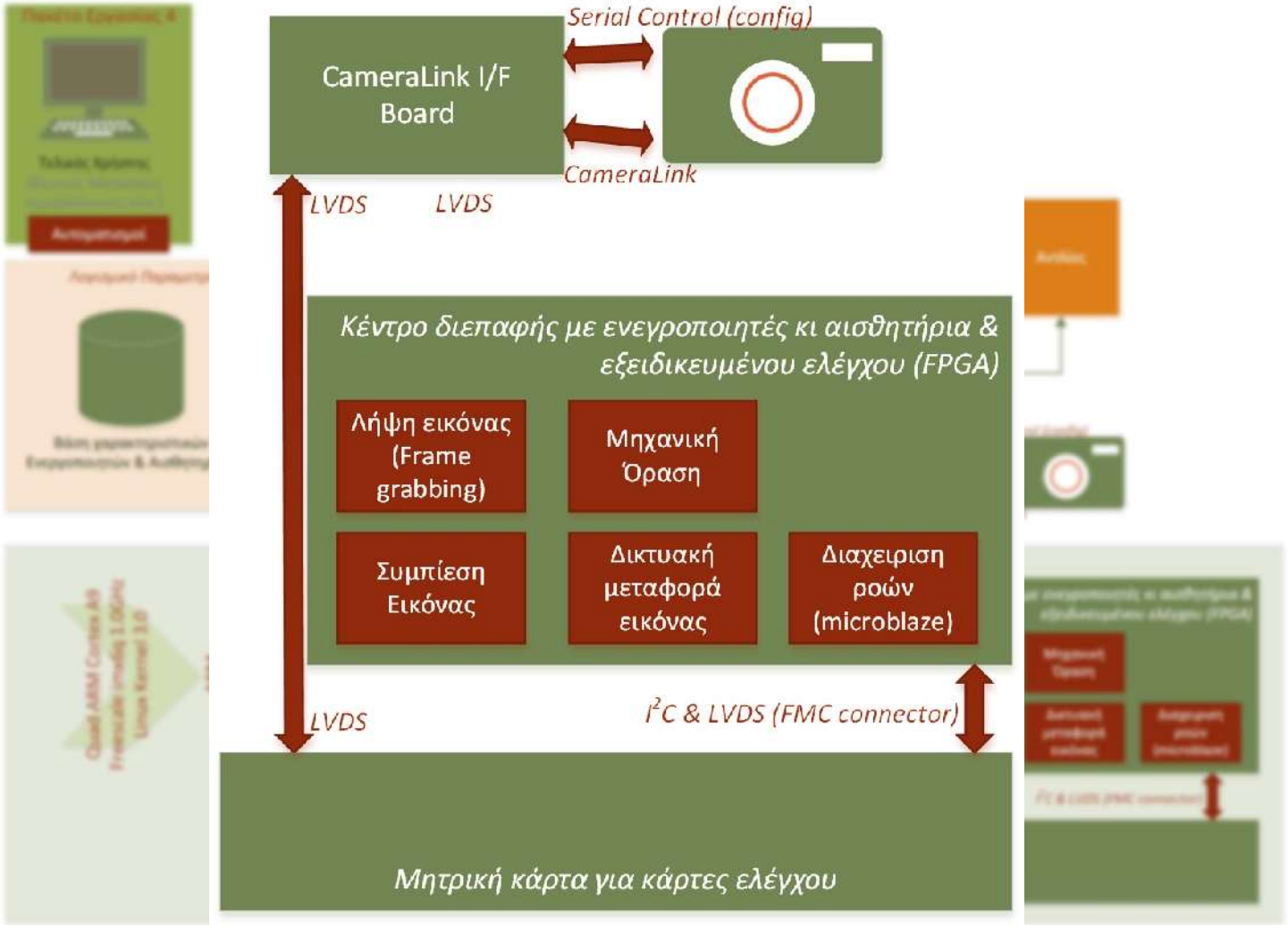
FPGA Architecture
(Control with Machine Vision)



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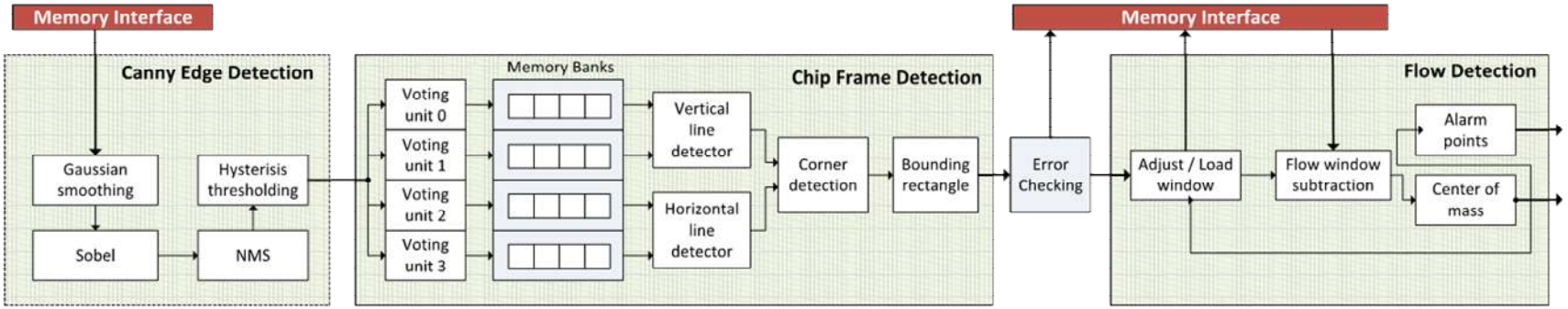
Machine Vision Processing Diagram

- 8bit grayscale uncompressed video
- 1Mpixel resolution
- Operational Frequency 170Mhz
- Processing time/frame 13.97ms (worst case)
- throughput 71.6fps (1Mpixel)
- 4-pixel parallel processing with pipelining



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Perfomance

	FF	LUT	BRAM	DSP	Time (ms)
Canny Edge Detection	7003	3053	13	-	1.55
Chip Frame Detection	3772	7563	24	28	12.34
Flow Detection	1581	1447	6	1	$77 \cdot 10^{-3}$
Machine Vision	12356	12063	43	29	13.97
LoC System	16094	16396	178	32	45 (*)
FF: Flip Flops, **LUT**: Look-Up-Tables, **BRAM**: 18Kbit Block RAM blocks, **DSP**: DSP48A1 slices					

(*) It may be decreased down to 15 ms after fine tuning.

Comparisons

Implementation	Platform	Algorithm	Frame Resolution (pixels)	Exec. Time/Frame (ms)	
Our Continuous Flow Machine Vision System	Spartan 6 FPGA	Canny Edge Detection	1024x1024	1.55	Total:13.94
		Hough Transform		12.34	
		Flow Identification		$77 \cdot 10^{-3}$	
Sappupo et al. [13]	AnaFocus ACE16kv2 FPP /Altera Nios II	CNN based implementation	128x128	90μs	
Demiris, Blionas [14]	CPU	Flow Detection	640x480	more than 35ms	
Texas Inst. [26]	DSP	Canny Edge Detection	1024x1024	18.5	
Ogawa, Ito, Nakano [27]	GPU	Canny Edge Detection	1024x10240	444.29	
Li, Jiang, Fan [28]	Virtex-5 FPGA	Canny Edge Detection	512x512	5.24	
Khan et al. [29]	DSP	Hough Transform	320x240	12	
Van Der Braak et al. [30]	GPU	Hough Transform	1920x1080	10.6	

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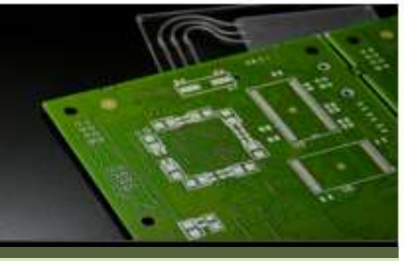

Point of Care System Validation - measurements

- Responce Time of the machine vision control loop ~45ms
- Responce Time of the control loop without the machine vision ~26.9ms
- Responce Time of the system valve – air circuit Dependence from the alarm point on the chip, the fluid speed and the quantity. For fast control typical value ~230ms.

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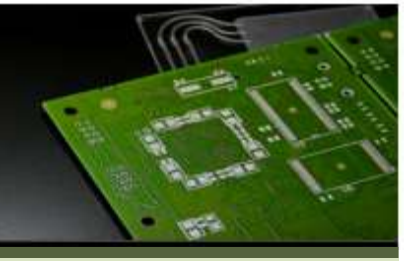

Point of Care System Validation – measurements after fine tuning

- Responce Time of the machine vision control loop ~15ms
- Responce Time of the control loop without the machine vision <1ms
- Responce Time of the system valve – air circuit Dependence from the alarm point on the chip, the fluid speed and the quantity <100ms

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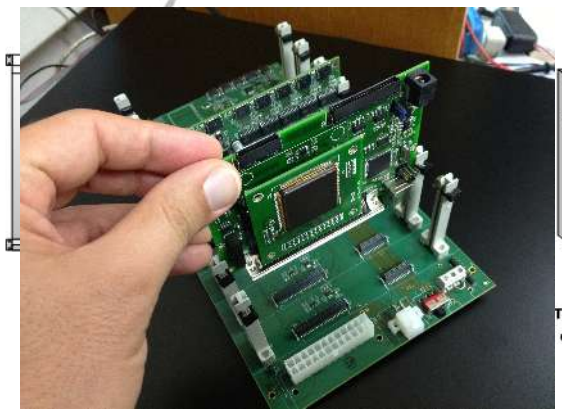
System Integration

Ευέλικτο λογισμικό:
Υποστήριξη & επέκτα
πειραμάτων από μη ε



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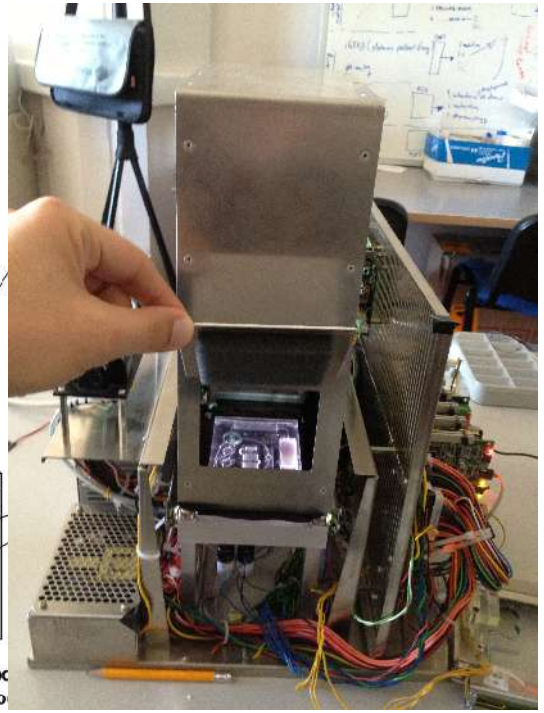

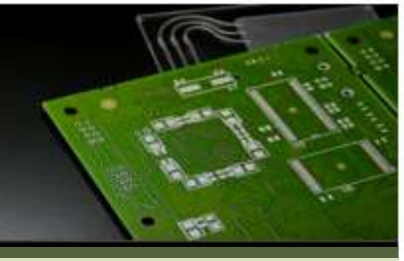

Implementation platform

- FPGA: Spartan 6 LX150T XC6SLX150T-3FGG676
- 128 MB DDR3 SDRAM x16
- Development Boards
- Avnet Spartan-6 LX150T Development Kit

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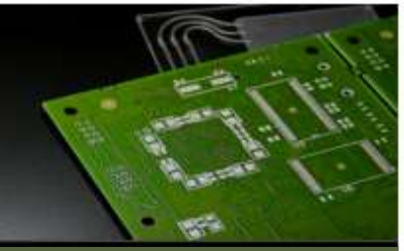
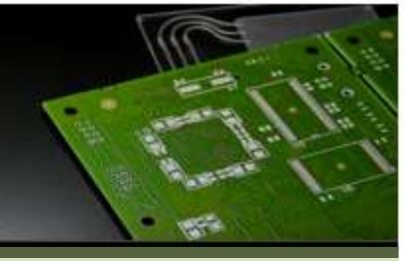
Final Implementation results after interconnections and placement for every implemented block

Module Name	Slices	Slice Reg	LUTs	LUTRAM	BRAM/FIFO	DSP48A1
system	1095/18699	0/31754	0/34307	0/1062	0/147	0/47
lmb_bram	0/0	0/0	0/0	0/0	0/32	0/0
system	0/0	0/0	0/0	0/0	0/0	0/0
clock_generator_0	0/0	0/0	0/0	0/0	0/0	0/0
dlmb	0/1	0/1	0/1	0/1	0/0	0/0
ilmb	0/1	0/1	0/1	0/1	0/0	0/0
microblaze_0	0/1024	0/1252	0/1494	0/139	0/4	0/3
xps_timer_0	0/115	0/198	0/147	0/0	0/0	0/0
xsvi2dma_bw	0/116	0/247	0/168	0/4	0/0	0/0
xps_intc_0	0/118	0/201	0/161	0/0	0/0	0/0
xsvi2dma	0/125	0/262	0/183	0/14	0/0	0/0
Soft_TEMAC	0/1323	0/2393	0/2208	0/74	0/19	0/0
MCB_DDR3	0/1431	0/2919	0/2608	0/448	0/5	0/0
mb_plb	0/155	0/94	0/252	0/0	0/0	0/0
proc_sys_reset_0	0/17	0/34	0/22	0/2	0/0	0/0
xsvi_mv_osd_0	0/1870	0/1371	0/4338	0/0	0/0	0/0
i2c_0	0/289	0/372	0/418	0/12	0/0	0/0
ilmb_cntlr	0/3	0/2	0/1	0/0	0/0	0/0
CamLink_FrameGrabber	0/35	0/63	0/73	0/0	0/0	0/0
jpege_udp	0/4618	0/8140	0/9809	0/14	0/45	0/12
dlmb_cntlr	0/5	0/2	0/3	0/0	0/0	0/0
machine_vision_0	0/5391	0/12243	0/10791	0/265	0/42	0/30
vdma_write_0	0/575	0/1202	0/1089	0/3	0/0	0/0
CSC_RGB2YCrCb	0/71	0/160	0/92	0/20	0/0	0/2
mdm_0	0/77	0/122	0/94	0/15	0/0	0/0
dvi2xsvi	0/8	0/26	0/23	0/23	0/0	0/0
RS232	0/83	0/126	0/112	0/11	0/0	0/0
FLASH_16Mx16	1/153	0/323	1/219	0/16	0/0	0/0



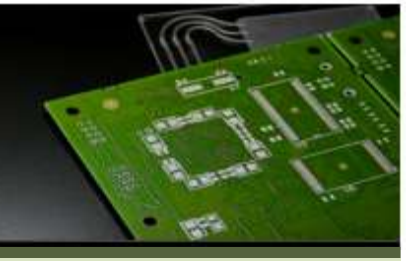
Final Implementation results after interconnections and placement for every FPGA element

Resource Type	Available	Required	Utilization (%)
LUT	92152	48220	53%
FD_LD	184304	34916	19%
SLICEL	6099	3192	53%
SLICEM	5420	2837	53%
SLICEX	11519	6028	53%
BSCAN	4	1	25%
BUFGMUX	16	11	69%
BUFIO2	32	2	7%
BUFIO2FB	32	1	4%
BUFPLL	8	1	13%
BUFPLL_MCB	4	1	25%
DSP48A1	180	51	29%
ILOGIC2	396	10	3%
IODELAY2	586	44	8%
MCB	4	1	25%
OLOGIC2	396	46	12%
PLL_ADV	6	3	50%
RAMB16BWER	268	143	54%
>RAMB16BWER		139	
>RAMB8BWER		8	
146	444	32.88%	



Lowering the cost

- Capability for implementation on FPGA of Spartan 6 LX family
  - § LX75 without any modification (30% cost reduction of FPGA)
  - § LX45 after small modifications for size reduction (50% cost reduction of FPGA).



Overall Performance

- The entire system and all blocks have been designed so to be compliant with the following performance:
  - § FPGA: Spartan 6 speed grade -3
  - § video 1MegaPixel@60fps over 1G network.